

JEDEC STANDARD

FBDIMM Specification: High Speed Differential PTP Link at 1.5 V

JESD8-18A

(Revision of JESD8-18, SEPTEMBER 2006)

MARCH 2008

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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FBDIMM HIGH SPEED DIFFERENTIAL PTP LINK AT 1.5 V

Introduction

This specification is a JEDEC standard for the point-to-point link for the Fully Buffered DIMM. It is the result of a large amount of work from many people and is derived from prior internal specifications used at Intel Corporation with feedback from external vendors and the JEDEC Fully-Buffered DIMM Link Signaling Task Group.

FBDIMM HIGH SPEED DIFFERENTIAL PTP LINK AT 1.5 V

(From JEDEC Board ballot JCB-06-01, JCB-06-60, JCB-06-61, and JCB-06-62, formulated under the cognizance of the JC-16 on Interface technology.)

1 Scope

This specification defines the high-speed differential point-to-point signaling link for FBDIMM, operating at the buffer supply voltage of 1.5V that is provided at the FBDIMM DIMM connector. This specification also applies to FBDIMM host chips which may operate with a different supply voltage. The link consists of a transmitter and a receiver and the interconnect in between them. The transmitter sends serialized bits into a lane and the receiver accepts the electrical signals of the serialized bits and transforms them into a serialized bit-stream. The first generation FBDIMM link is being specified to operate from 3.2 to 4.8 Gb/s. The specifications are defined for three distinct bit-rates of operation: 3.2 Gb/s, 4.0 Gb/s and 4.8 Gb/s.

The link utilizes a derived clock approach and transmitter de-emphasis to compensate for channel loss characteristics. The link definition has the flexibility to accommodate future silicon enhancement circuits such as forwarded clocking or advanced equalization techniques to meet future signaling targets.

1.1 Structure

The specification is defined in four sections, covering the general signaling specifications for the silicon I/O:

Section 1 covers the scope of the document, and defines important terms.

Section 2 lists key reference documents.

Section 3 defines important terms.

Section 4 defines the interface requirements and is divided into four subsections:

Section 4.1 defines the clocking requirements.

Section 4.2 defines common requirements for both transmitter and receiver.

Section 4.3 defines requirements that are unique to the transmitter.

Section 4.4 defines requirements that are unique to the receiver.

Section 5 defines measurement and compliance testing procedures.

The interconnect between transmitter and receiver is not directly specified but implied by the difference between receiver and transmitter specifications. The interconnect needs to have a smooth enough characteristic to be operational at the frequencies which it is intended to support.

1.2 Interconnect Definition

The overall budget for voltage and timing margins are divided into transmitter (TX), interconnect, and receiver (RX) specifications. The link signaling specifications defines the TX and RX requirements at the package pins. In the context of this specification, the interconnect consists of everything between the pins at a transmitter package and the pins of a receiver package. The interconnect components in FBDIMM are socket(s) (if used), PCB (printed circuit board(s)) and connector(s).

Interconnect voltage and timing budgets are derived from the output specifications of the TX and the input specifications for the RX. Note that the TX and RX termination (specified in Table 4.3 and Table 4.4) and the test load are $50\ \Omega$ (specified in Section 5). Figure 1.1 depicts the compliance measurement points to capture each portion of the budget. The transmitter and receiver parameters are defined into test loads. This methodology ensures that the channel interactions are not included in the TX and RX measurement.

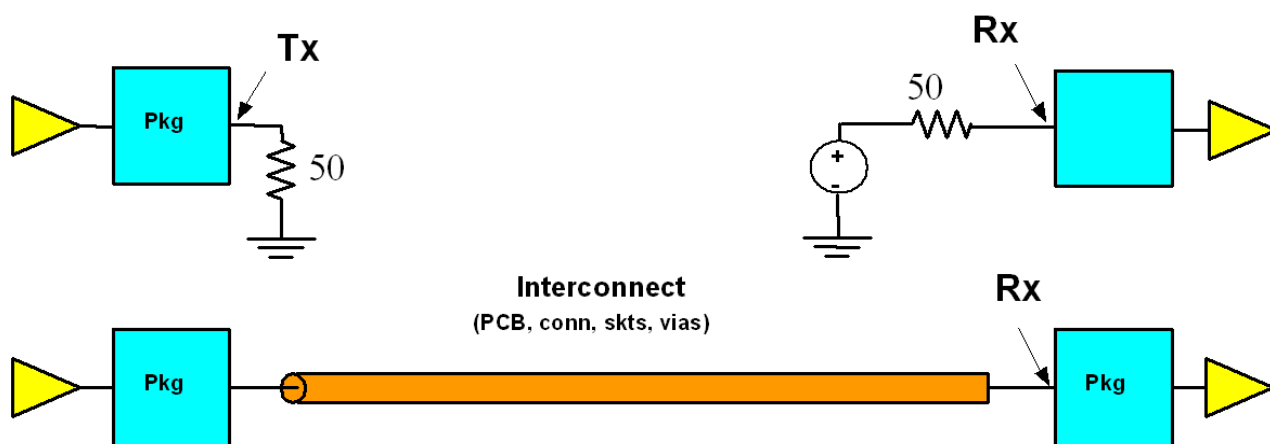


Figure 1.1 — TX to RX Connection

The transmitter, receiver, and reference clock specifications presented in Section 4 have been derived based on analysis of two specific interconnects: a host-to-first-DIMM interconnect and a DIMM-to-DIMM interconnect. The interconnect descriptions provided below are not intended to be used as a design specification. System designers must perform thorough analysis of any proposed FBD interconnect.

The interconnect model used to analyze the host-to-first-DIMM configuration has the following components:

- MB trace (host to connector): 3.0 to 12.0 inches
- Optional riser card trace: connector to connector: 2.0 to 5.0 inches
- DIMM trace (DIMM connector to AMB): 0.33 to 2.0 inches

The interconnect model used to analyze the DIMM-to-DIMM configuration has the following components:

- DIMM trace (AMB to DIMM connector): 0.33 to 2.0 inches
- Motherboard trace: connector to connector: 0.5 to 2.0 inches
- DIMM trace (DIMM connector to AMB): 0.33 to 2.0 inches

1.2 Interconnect Definition

The analysis was performed assuming FR4 PCB dielectric for both motherboard and DIMM; the differential impedance (Z_{DIFF}) was $85\ \Omega \pm 15\%$ for motherboard and DIMM stripline traces and was $85\ \Omega \pm 20\%$ for DIMM microstrip traces. Note that using the above description as a system design recipe is not enough to guarantee a working channel. The range of achievable lengths may be narrower or wider than the above, depending on materials, stackups, trace geometries, and other design choices.

2 References

The following documents contain provisions that, through references in this text, constitute provisions of this specification. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this specification are encouraged to investigate the possibility of applying the most recent editions of the referenced documents below. For undated references, the latest edition of the document referred to applies.

JEDEC JC-40, FBDIMM Architecture and Protocol Draft Specification

INTEL, FBD240 Connector Draft Specification

JEDEC JC-40, Advanced Memory Buffer Design Draft Speciation

JEDEC JC-45, FB4300/5300/6400 DDR Fully Buffered DIMM Design Specification

JEDEC MO-256B, Fully Buffered Dual Inline Memory Module Family. (Module Outline)

JEDEC SO-003, FBDIMM Socket Outline

JEDEC JESD22A114, Electrostatic Discharge (ESD) Sensitivity Testing (HBM)

3 Terms and Definitions

3.1 D+ and D-

The D+ and D- terms used in this document are used to indicate the two conductors or signals of a differential signaling pair.

3.2 Lane

One differential pair in one direction, consisting of a D+ and a D- conductor.

3.3 Port

In physical terms, a group of transmitters and receivers physically located on the same chip that define a Link.

3 Terms and Definitions (cont'd)

3.4 Link

A dual-simplex communications path between two components. The collection of two Ports and their interconnecting Lanes.

3.5 Differential Signaling

A Differential Signal is defined by taking the voltage difference between two conductors. In this specification, a differential signal or differential pair is comprised of a voltage on a positive conductor, **VD+**, and a negative conductor, **VD-**. The differential voltage (**VDIFF**) is defined as the difference of the positive conductor voltage and the negative conductor voltage (**VDIFF = VD+ - VD-**). The Common Mode Voltage (**VCM**) is defined as the average or mean voltage present on the same differential pair (**VCM = [VD+ + VD-]/2**).

This document's electrical specifications often refer to peak-to-peak measurements or peak measurements, which are defined by the following equations.

VDIFFp-p = (2*max|VD+ - VD-|) (This applies to a symmetric differential swing)

VDIFFp-p = (max|VD+ - VD-| {VD+ > VD-} + max|VD+ - VD-| {VD+ < VD-}) (This applies to an asymmetric differential swing.)

VDIFFp = (max|VD+ - VD-|) (This applies to a symmetric differential swing)

VDIFFp = (max|VD+ - VD-| {VD+ > VD-}) or (max|VD+ - VD-| {VD+ < VD-}) which ever is greater (This applies to an asymmetric differential swing.)

VCMp = (max|VD+ + VD-|/2)

NOTE The maximum value is calculated on a per unit interval evaluation. The maximum function as described is implicit for all peak-to-peak and peak equations throughout the rest of this section, and thus a max function will not appear in any following representations of these equations.

In this section, DC is defined as all frequency components below Fdc = 30 kHz. AC is defined as all frequency components at or above Fdc = 30 kHz. These definitions pertain to all voltage and current specifications.

An example waveform is shown in Figure 3.1. In this waveform the differential peak-peak signal is approximately 0.6 V, the differential peak signal is approximately 0.3 V and the common mode is approximately 0.25 V.

3 Terms and Definitions (cont'd)

3.5 Differential Signaling

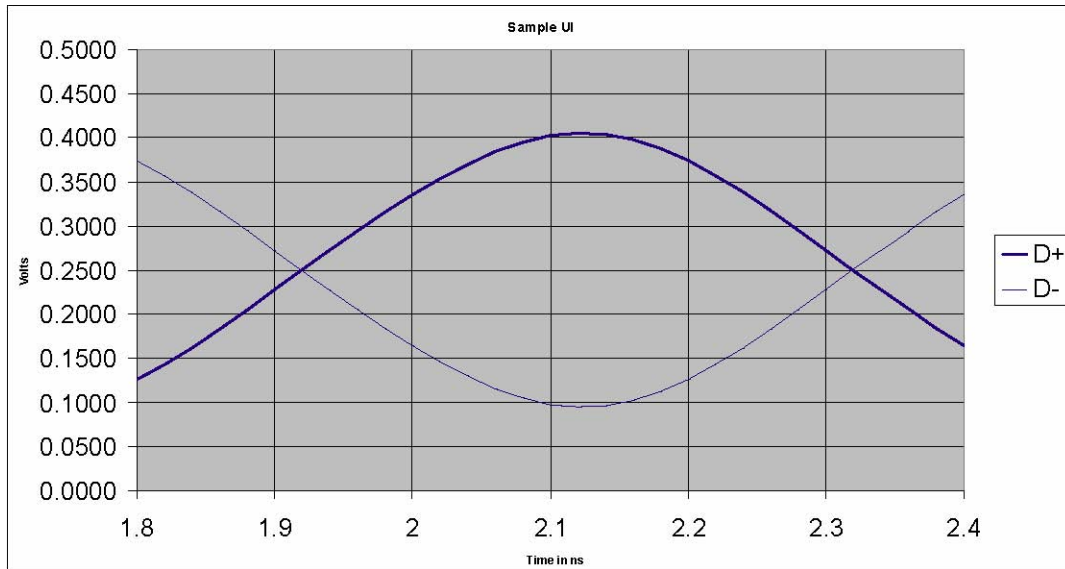


Figure 3.1 — Sample Differential Signal

3.6 Unit Interval (UI)

Given a <...1010...> data pattern, the Unit Interval is the value measured by averaging the time interval between voltage transitions, over a time interval long enough to make all intentional frequency modulation of the source clock negligible. The UI will be different depending on the data rate of operation.

3.7 Transition Density in Transmitted Signals

The FBDIMM link doesn't prescribe encoding. However the link bit stream needs to maintain a minimum transition density. The transition density is defined as the number of transitions that occurs either from 0 to 1 or from 1 to 0 within any bit stream of a prescribed length. The minimum prescribed transition density Transition-Density_min is:

6 transitions per 512 bits: FBDIMM at 3.2 Gb/s, 4.0 Gb/s and 4.8 Gb/s

The prescribed minimum is required to enable phase tracking of the received data by the receiver while at the same time minimize the overhead requirements.

3 Terms and Definitions (cont'd)

3.8 Jitter and BER

Jitter is defined as the deviation in the edges of a sequence of data bits from their ideal timing positions. This deviation can be in phase, period or duty cycle. Jitter is further categorized into random jitter and deterministic jitter. The total jitter is the convolution of the probability density for all the independent jitter sources. The random jitter magnitude can be approximated as Gaussian and can be used to estimate the bit error ratio (BER) of the link. In this document the allocation to random jitter and deterministic jitter has not been separately specified. The total jitter must support a maximum BER of 10^{-12} . The methods for measuring BER compliance are still being evaluated.

3.9 De-emphasis

De-emphasis is the engineering term used to describe the technique of utilizing a voltage swing reduction of non-transition bits. Figure 3.2 shows an example of a de-emphasized differential signal. De-emphasis is different from pre-emphasis in that non-transition bits are reduced in voltage as opposed to an increase in voltage swing for transition bits with pre-emphasis. De-emphasis is included to minimize Inter-symbol interference (ISI) due to the difference in loss across the frequency band where the main energy of the transmitted bit patterns is located. De-emphasis must be implemented when multiple bits of the same polarity are output in succession. Subsequent bits are driven at a differential voltage level below the first bit and individual bits are always driven at the full voltage level, for normal operation.

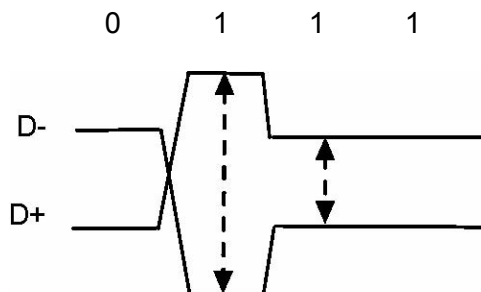


Figure 3.2 — De-emphasis

3.10 Electrical Idle (EI)

The condition when both conductors of a differential pair are at 0 volt (grounded) level. Electrical idle is primarily used in power saving and inactive states (i.e., DISABLE).

3.11 Reference Clock

The reference clock network consists of the clock generator and the clock buffer that drives the PLL of any front-end transmitter or receiver. The same reference clock shall be transmitted to the front-end of the chips at both ends of the link. The reference clock signal shall meet the High-Speed Current Steering Logic (HCSL) specification.

3 Terms and Definitions (cont'd)

3.12 Front-End Transmitter and Receiver

The differential transmitter consists of pre-driver, driver and package signal traces ending at the package pin. The receiver consists of the input package pins and signal traces leading to the input sampling amplifier, recovery circuit for the sampling clock phases and appropriate deskew circuits for passing the received data to the back-end. A depiction is in Figure 3.3.

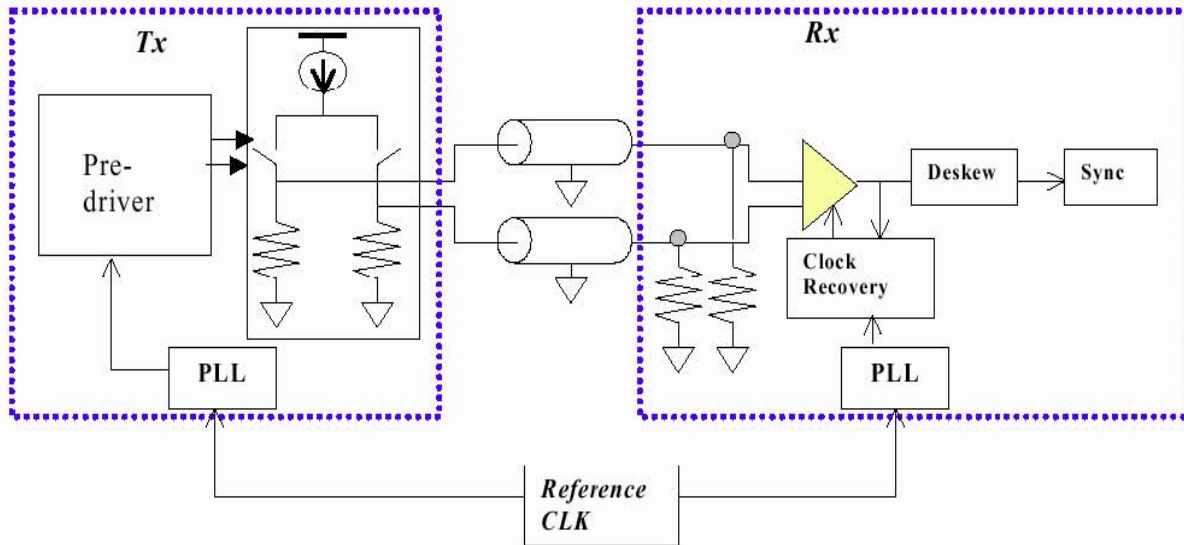


Figure 3.3 — TX to RX Connection

Figure 3.3 shows an example of the connection for one lane at the TX-RX level. The appropriate phase of the receiver end sampling clock is derived from the transmitted data. The connection between the two physical layer front-ends is DC coupled.

The following rules shall be obeyed by the link:

- 1) The transmitter output and the receiver input is VSS referenced.
- 2) Each TX-RX bit connection between two components through the interconnect channel must be DC coupled.
- 3) The signal stream from TX-RX shall maintain a minimum transition density Transition-Density_min (specified earlier).

Additional specifications for the transmitter front-end and the receiver front-end are in Section 4.

3 Terms and Definitions (cont'd)

3.13 List of Abbreviations and Definitions

This document uses the following abbreviations and definitions:

Abbreviation	Definition
AC	Alternating Current
AMB	Advanced Memory Buffer
BER	Bit Error Ratio
BIST	Built-in Self Test
CAL	Crosstalk Aggressor Lane: any lane that can influence the Lane Under Test (other than itself)
CDF	Cumulative Distribution Function
CDR	Clock and Data Recovery
CM	Common Mode
dB	Decibel .One tenth of the common logarithm of the ratio of relative powers, equal to 0.1 B (bel)
DC	Direct Current
DDJ	Data Dependent Jitter: a bounded distribution of jitter, with amplitude fully correlated to the data pattern sampling it, measured by its peak-to-peak value for a given pattern
DIMM	Dual Inline Memory Module
DJ	Deterministic Jitter: an even distribution of jitter, measured by its effective mean shift on a convolved Gaussian Jitter
DUT	Device Under Test: the AMB component that is being tested
EI	Electrical idle, where both conductors of a differential pair are at VSS level
EMI	Electro Magnetic Interference
End components	Components at either end of the FBDIMM channel, i.e. the host and the last AMB
ESD	Electro Static Discharge
FB(D)	Fully-Buffered (DIMM)
HCSL	High-speed Current Steering Logic
Host	Memory controller agent on an FBDIMM channel
Intermediate components	Any FBDIMM component that is not at either end of the channel
Interconnect	
ISI	Inter Symbol Interference
MEMBIST	Memory Built-in Self Test
Mesochronous	Same frequency with unknown (but fixed) phase relationship
Northbound	The direction of signals running from the furthest DIMM toward the host
JEDEC	JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)
LUT	Lane Under Test: the lane for which the specification is being validated
PDF	Probability Density Function
PLL	Phase Locked Loop

3 Terms and Definitions (cont'd)

3.13 List of Abbreviations and Definitions (cont'd)

Abbreviation	Definition
PTP	Point To Point
PTH	Plated Through-Hole
PVT	Process, Voltage and Temperature
rad/s	Radians per second. Unit of angular frequency measure
RJ	Random Jitter: an unbounded Gaussian distributed jitter, defined by its RMS variance
RX	Receiver
SE	Single Ended
SI	Signal Integrity
Simplex	Simplex means that communication can only flow in one direction
SJ	Sinusoidal Jitter: a jitter distribution caused by a sinusoidal amplitude modulation
Southbound	The direction of signals running from the host controller toward the DIMMs
SSC	Spread Spectrum Clocking. Utilized to lower EMI.
SSO	Simultaneously Switching Outputs
TP_AMB	Test Point AMB: the ball of the AMB package
TX	Transmitter
UI	Unit Interval. Time period per data bit.
VSS	Ground (0V)
99.7% Confidence Level	Defines that the result derived from a measurement, is a confidence interval in which a measurement or trial falls corresponding to a probability of 99.7%. The confidence interval of interest is symmetrically placed around the mean.

NOTE The terms host, chipset and memory controller are used interchangeably throughout the rest of this document. The term motherboard is used as a generic term to describe the PCB onto which the memory controller is mounted. Actual implementations could have distributed memory controllers mounted on separate boards.

4 Specification Details

4.1 Clocking Specifications

4.1.1 HCSL reference clocks

To reduce jitter and allow for future silicon fabrication process changes, HCSL (High-Speed Current Steering Logic) clocks are used, as illustrated in Figure 4.1. The nominal single-ended swing for each clock is 0 to 0.7 V. The same system clock shall be transmitted to the two components at the ends of the link, if necessary, through connector(s).

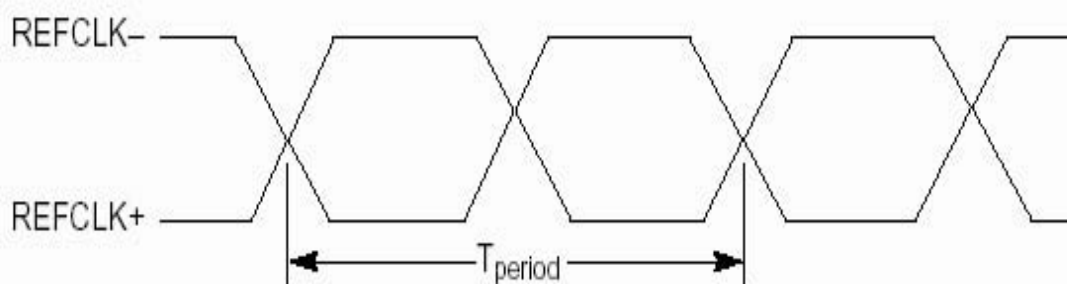


Figure 4.1 — Differential Reference CLK Waveforms

The reference clock frequency is 1/24 of the link data rate, e.g., 166.67 MHz for a data rate of 4.0 Gb/s. The reference clock pair is routed point-to-point to each device from the system board.

The FBDIMM channel utilizes mesochronous clocking, i.e., the phase relationship between TX reference clock and RX reference clock is unspecified. However, in order to limit the jitter difference between TX and RX there is an upper limit for the phase difference between data and reference clock at the RX (also known as the transport delay, specified in Table 4.1).

The clocks must be routed according to best-known clock routing rules for SI and EMI performance. The routing of each signal in any given clock pair between the clock source and the connector must be well matched in length (< 5 mils) and appropriately spaced away from other non-clock signals to avoid excessive crosstalk.

4.1.2 Reference Clock Frequency Tolerance

The frequency of the reference clock has a static tolerance, and a temporal variation. This temporal part varies due to the spread spectrum modulation and due to the mean period of the phase noise over different periods of integration.

The implementation of the multiplying PLL in the AMB should be aware that the frequency tracking capabilities of the integrated VCO should be capable of following the mean period variation. For example as the forward tracking bandwidth of PLL is increased, then the variation of the mean period will increase. As the bandwidth requirements of the PLL are well defined within the standard, it is possible to define exactly the expected maximum frequency tracking requirements of the VCO.

4.1 Clocking Specifications (cont'd)

4.1.2 Reference Clock Frequency Tolerance (cont'd)

To be able to measure the maximum tracking frequency, the reference clock phase is filtered by an equivalent 2nd order PLL transfer function represents the worst case, i.e., maximum bandwidth and maximum peaking, in the frequency domain. [Need to fix subscripts in equation below]:

$$\frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2} \quad (4.1)$$

After multiplying these frequency domain filters by the reference clock phase jitter spectrum, the spectra is converted back into the time domain, and the maximum instantaneous frequency is measured. To ensure that a true peak value has been calculated, sufficient edge samples must be used to ensure that the filtered underlying random source has reached a peak value for the link's target BER.

The methods used to implement the measurement of reference clock jitter are beyond the scope of this specification, any testing method may be used that will provide a mathematically equivalent result. This function is not meant as a requirement for an implementation. It is used as a bounding function for modeling purposes to establish the limits for the f_{3dB} frequency and the maximum peaking. Other implementations that can meet at least the roll off and limit the peaking given by this function are also acceptable.

The temporal variation referred to above is specified in Table 4.1 as the “reference clock dynamic frequency,” or $f_{Refclk-dyn}$. Table 4.2 indicates how this dynamic frequency range differs from the absolute frequency range.

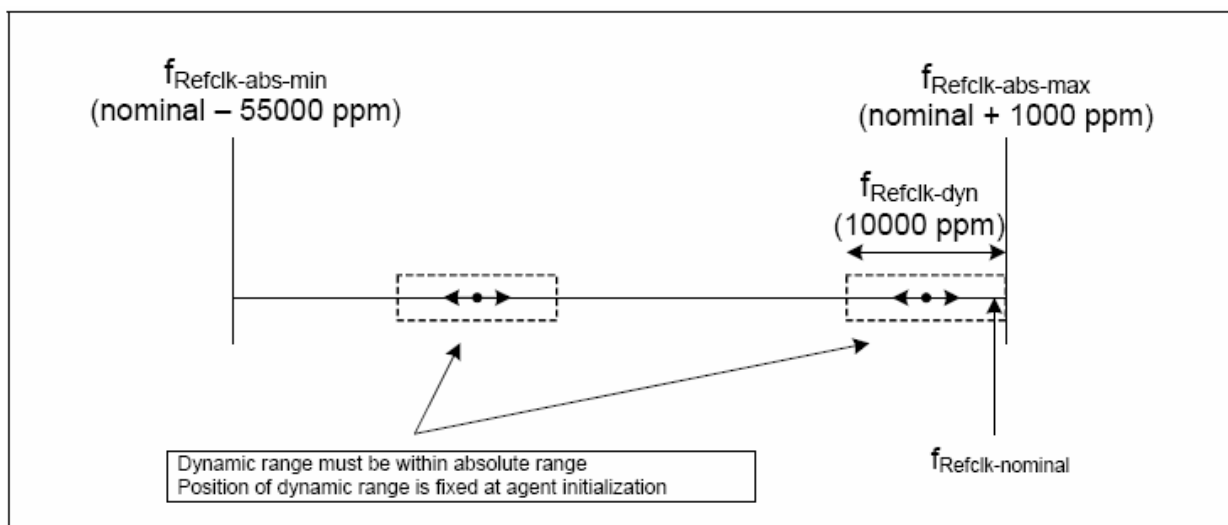


Figure 4.2 — Reference Clock Absolute and Dynamic Ranges

4.1 Clocking Specifications (cont'd)

4.1.3 Spread Spectrum Clocking (SSC)

Spread Spectrum Clock (SSC) with up to -0.5% down spread in frequency shall be supported. The frequency of the clock and therefore bit rate can be modulated from 0% to -0.5% of the nominal data rate/frequency, at a modulation rate in the range between 30 kHz and 33 kHz. The modulation profile of SSC shall be able to provide optimal or close to optimal EMI reduction. Typical profiles include triangular or “Hershey kiss” profile.

4.1.4 Reference Clock Jitter Spectrum

Different devices may have different phase jitter¹ tracking behaviors due to variation of the jitter transfer function of their PLLs, transport delays between transmitter and receiver, and differences in the propagation delays in the devices. In order for the FBDIMM channel function properly when the transmitter and receiver utilize devices with different phase jitter tracking behavior, a specification of the reference clock jitter spectrum is necessary.

To be able to measure jitter¹ on the reference clock and translate this directly into a data eye closure at the receiver, the reference clock phase jitter is filtered by a phase jitter transfer function that represents the worst case mismatch between transmitter and receiver phase tracking. Figure 4.3 shows the four filter functions defined for 4.8 Gb/s. After multiplying these frequency domain filters by the reference clock phase jitter spectrum, the SSC from the reference clock is separated from the spectrum. After converting these spectra back into the time domain, peak-to-peak amplitude of the SSC spectrum and the RMS of the remaining spectrum is measured, and the maximum is then found for the four filter functions. To ensure that a stable RMS of the spectrum is calculated, sufficient edge samples must be used to ensure that the RMS is valid at the link's target BER.

The methods used to implement the measurement of reference clock jitter are beyond the scope of this specification, any testing method may be used that will provide a mathematically equivalent result.

¹ Phase jitter is defined as the difference between the actual position of a clock edge and the edge of an ideal clock whose period is constant and is the average period of clock being measured.

4.1 Clocking Specifications(cont'd)

4.1.4 Reference clock Jitter Spectrum (cont'd)

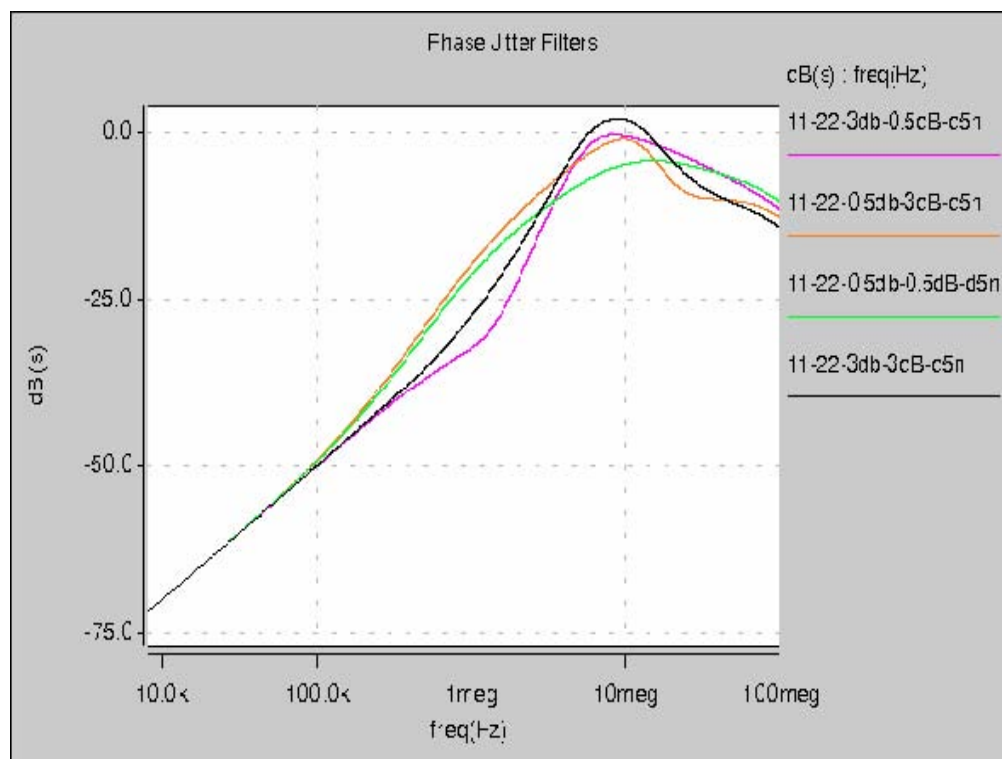


Figure 4.3 — Phase Jitter Filter for Reference Clocks

The specification uses a second-order PLL transfer function to approximate the jitter transfer function of a device's PLL. Actual PLLs used in typical CMOS processes are sampled systems often using third-order or higher order transfer functions. However, they can all be approximated by a second-order transfer function. The transfer function assuming second order PLLs is defined by the following s domain equation:

$$H(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} e^{-sT_D} - \frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2} \right] \quad (4.2)$$

In this equation, ζ_1 and ζ_2 are the damping factors for PLL 1 and 2, and ω_{n1} and ω_{n2} are the natural frequencies for PLL 1 and 2. The variable T_D represents the total transport delay measured from the sample clock to the data measured around the loop through Rx PLL, clock distribution delays, Tx PLL, and TX data flight time (see Figure 4.9).

This function is not meant as a requirement for an implementation. It is used as a bounding function for modeling purposes to establish the limits for the f_{3dB} frequency and the maximum peaking. Other implementations that can meet at least the roll off and limit the peaking given by this function are also acceptable.

4.1 Clocking Specifications(cont'd)

4.1.5 Summary of Reference Clock Input Specifications

The transmission line between the device driving the reference clock driver the FBDIMM agent may be optionally terminated on die. Reference clock voltage level specifications in Table 4.1 assume an unterminated transmission line. Levels for the on-die termination case will be specified in a future release.

Table 4.1 — Summary of Reference Clock Input Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
$f_{\text{Refclk-3.2}}$	Reference clock frequency @ 3.2 Gb/s (nominal 133.33 MHz)	126.00	133.46	MHz	1, 2, 3
$f_{\text{Refclk-4.0}}$	Reference clock frequency @ 4.0 Gb/s (nominal 166.67 MHz)	157.50	166.84	MHz	1, 2, 3
$f_{\text{Refclk-4.8}}$	Reference clock frequency @ 4.8 Gb/s (nominal 200 MHz)	189.00	200.20	MHz	1, 2, 3
$f_{\text{Refclk-dyn}}$	Reference clock dynamic frequency		10,000	ppm	4
V_{max}	Single-ended maximum voltage		1.15	V	5, 7
V_{min}	Single-ended minimum voltage	-0.3		V	5, 8
$V_{\text{Refclk-diff-ih}}$	Differential voltage high	150		mV	6
$V_{\text{Refclk-diff-il}}$	Differential voltage low		-150	mV	6
V_{Cross}	Absolute crossing point	250	550	mV	5, 9, 10
$V_{\text{Cross-delta}}$	V_{Cross} variation		140	mV	5, 9, 11
$V_{\text{Refclk-cm-acp-p}}$	AC common mode		225	mV	12
$ER_{\text{Refclk-diffRise}},$ $ER_{\text{Refclk-diff-Fall}}$	Rising and falling edge rates	0.6	4.0	V/ns	6, 13
$ER_{\text{Refclk-Match}}$	% mismatch between rise and fall edge rates		?	%	6, 14
$T_{\text{Refclk-Dutycycle}}$	Duty cycle of reference clock	40	60	%	6
$V_{\text{RB-diff}}$	Ringback voltage threshold	-100	100	mV	6, 15
T_{Stable}	Allowed time before ringback	500		ps	6, 15
$I_{\text{I_CK}}$	Clock leakage current	-10	10	μA	16, 17
$C_{\text{I_CK}}$	Clock input capacitance	0.5	2.0	pF	17

4.1 Clocking Specifications(cont'd)

4.1.5 Summary of Reference Clock Input Specifications (cont'd)

Table 4.1 — Summary of Reference Clock Input Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
$C_{I_CK(\Delta)}$	Clock input capacitance delta	-0.25	0.25	pF	Difference between RefClk and RefClk# input capacitance
ω_{n1}	Natural frequency PLL1	$5.92 \cdot 2\pi$		Mrad/s	18, 19
Z_1	Damping factor PLL1	0.54	1.75		18
ω_{n2}	Natural frequency PLL2 (3.2 and 4.0 Gb/s link speeds)		$17.7 \cdot 2\pi$	Mrad/s	18, 20
$\omega_{n2-4.8}$	Natural frequency PLL2 (4.8 Gb/s link speed)		$11.8 \cdot 2\pi$	Mrad/s	18, 21
Z_2	Damping factor PLL2	0.54	1.75		18
T_D	Transport delay		5	ns	18, 22
N_{SAMPLE}		10^{12}		periods	23
$T_{REF-JITTER-RMS}$	Reference clock jitter (rms), filtered (3.2 and 4.0 Gb/s link speeds)		3.0	ps	24, 25
$T_{REF-JITTER-RMS-4.8}$	Reference clock jitter (rms), filtered (4.8 Gb/s link speed)		2.5	ps	24, 25
$T_{REF-SSCp-p}$	Reference clock jitter (peak-to-peak) due to spread spectrum clocking effects		30	ps	
$T_{REF-JITTER-DELTA}$	Reference clock jitter difference between adjacent AMBs		TBD	ps	

NOTE 1 The nominal reference clock frequency is determined by the data frequency of the link divided by 2 times the fixed PLL multiplication factor for the FBDIMM channel (6:1). $f_{data} = 2000$ MHz for a 4.0Gbps FBDIMM channel and so on.

NOTE 2 Measured with SSC disabled. Enabling SSC will reduce the reference clock frequency as described in 4.1.3.

NOTE 3 Not all FBDIMM agents will support all frequencies; compliance to the frequency specifications is only required for those data rates that are supported by the device under test.

NOTE 4 Defined as the range over which the reference clock frequency may vary during operation, using initialization of the FBDIMM agent as the starting point (see 4.1.2 and Figure 4.2 in particular). Specification includes the effects of spread spectrum modulation.

NOTE 5 Measurement taken from single-ended waveform.

NOTE 6 Measurement taken from differential waveform.

NOTE 7 Defined as the maximum instantaneous voltage including overshoot. See Figure 4.4.

NOTE 8 Defined as the minimum instantaneous voltage including undershoot See Figure 4.4.

4.1 Clocking Specifications(cont'd)

4.1.5 Summary of Reference Clock Input Specifications (cont'd)

NOTE 9 Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 4.4.

NOTE 10 Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 4.4.

NOTE 11 Defined as the total variation of all crossing voltages of rising REFCLK+ and falling REFCLK-. This is the maximum allowed variance in for any particular system. See Figure 4.5.

NOTE 12 The majority of the reference clock AC common mode occurs at high frequency (i.e., the reference clock frequency).

NOTE 13 Measured from -150 mV to + 150 mV on the differential waveform. The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential 0 V crossing. See Figure 4.6.

NOTE 14 Edge rate matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ± 75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median crosspoint is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations. The rising edge rate of REFCLK+ should be compared to the falling edge rate of REFCLK-. The maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 4.7.

NOTE 15 See Figure 4.8. T_{stable} is the time the differential clock must maintain a minimum ± 150 mV differential voltage after rising / falling edges before it is allowed to droop back into the ± 100 mV differential range.

NOTE 16 Measured with a single-ended input voltage of 1V.

NOTE 17 Applies to RefClk and RefClk#.

NOTE 18 This parameter is not a direct clock output parameter but it indirectly determines the clock output parameter $T_{\text{REF-JITTER}}$.

NOTE 19 Implies a -3 dB bandwidth of 11 MHz and jitter peaking of 3 dB.

NOTE 20 Implies a -3 dB bandwidth of 33 MHz and jitter peaking of 3 dB.

NOTE 21 Implies a -3 dB bandwidth of 22 MHz and jitter peaking of 3 dB.

NOTE 22 The net transport delay is the difference in time of flight between associated data and clock paths. The data path is defined from the reference clock source, through the TX, to data arrival at the data sampling point in the RX. The clock path is defined from the reference clock source to clock arrival at the same sampling point. See Figure 4.9. The path delays are caused by copper trace routes, on-chip routing, on-chip buffering, etc. They include the time-of-flight of interpolators or other clock adjustment mechanisms. They do *not* include the phase delays caused by finite PLL loop bandwidth because these delays are modeled by the PLL transfer functions.

NOTE 23 Direct measurement of phase jitter records over N_{SAMPLE} periods may be impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and the total jitter at N_{SAMPLE} samples extrapolated from an estimate of the sigma of the random jitter components. For details on this measurement, refer to 5.6.

NOTE 24 Measured with SSC enabled on reference clock generator.

NOTE 25 As “measured” after the phase jitter filter. This number is separate from the receiver jitter budget that is defined by the $T_{\text{RX-Total-MIN}}$ parameters.

NOTE 26 This maximum value is below the noise floor of some test equipment

4.1 Clocking Specifications(cont'd)

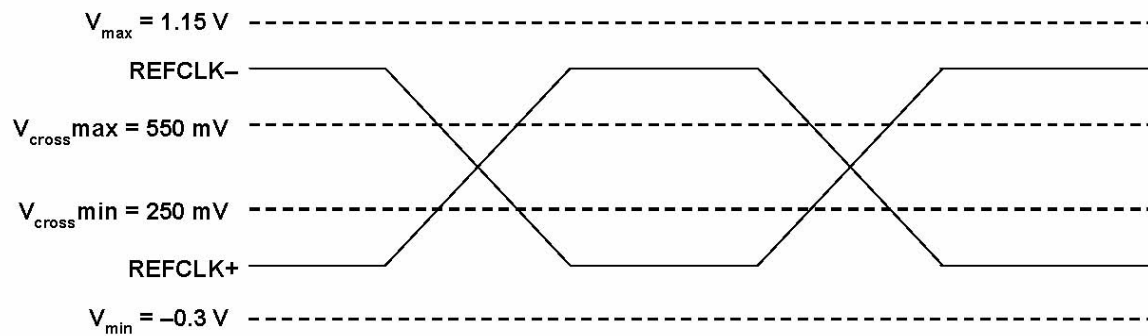


Figure 4.4 — Single-ended Maximum and Minimum Levels and V_{cross} Levels

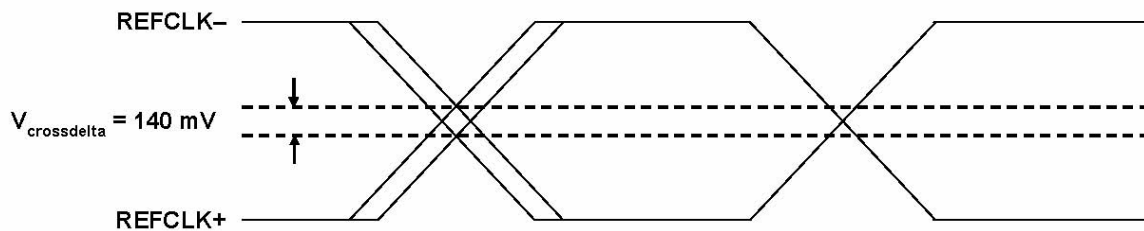


Figure 4.5 — $V_{\text{cross-delta}}$ Definition

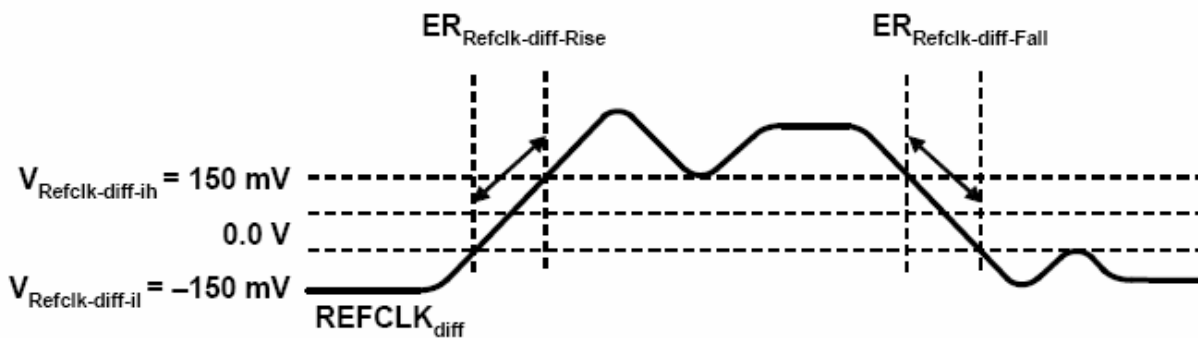


Figure 4.6 — Differential Edge Rate Definition

4.1 Clocking Specifications(cont'd)

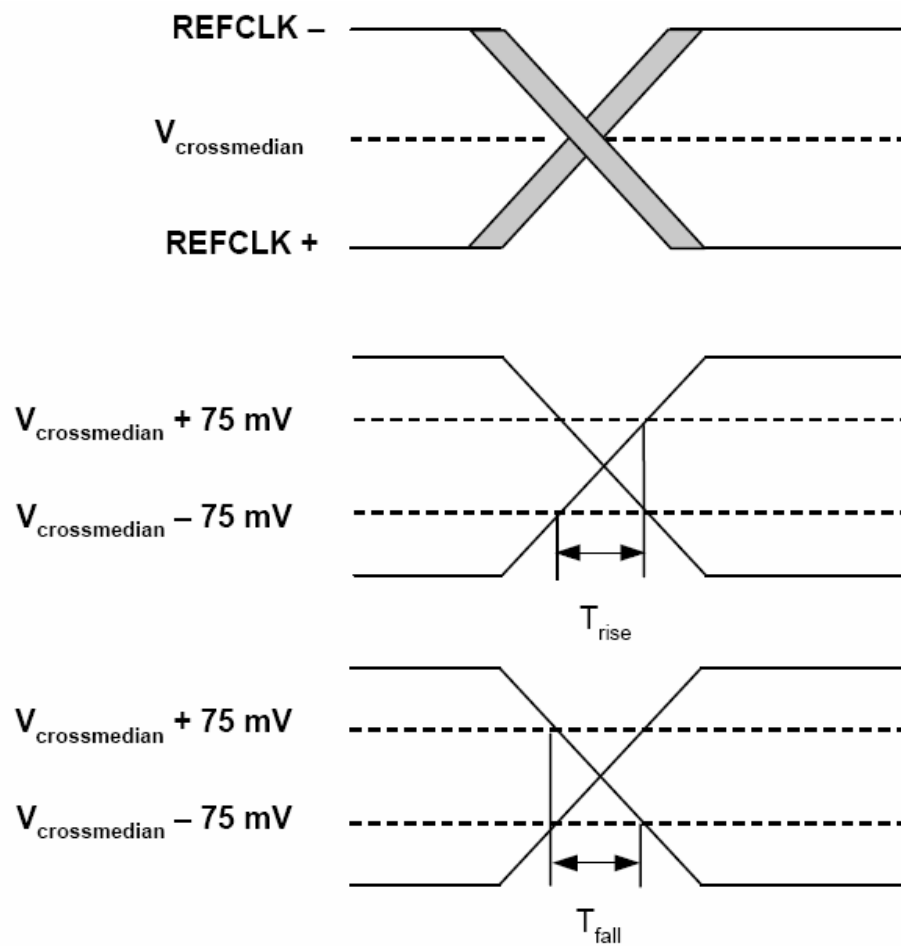


Figure 4.7 — Rise and Fall Time Definition (for $ER_{Refclk--Match}$ only)

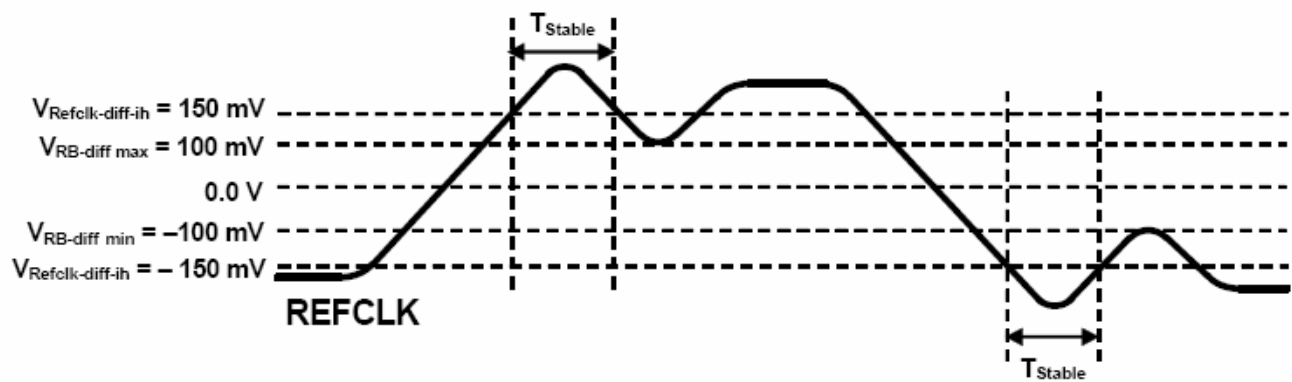


Figure 4.8 — $V_{RB-diff}$ and T_{Stable} Definitions

4.1 Clocking Specifications(cont'd)

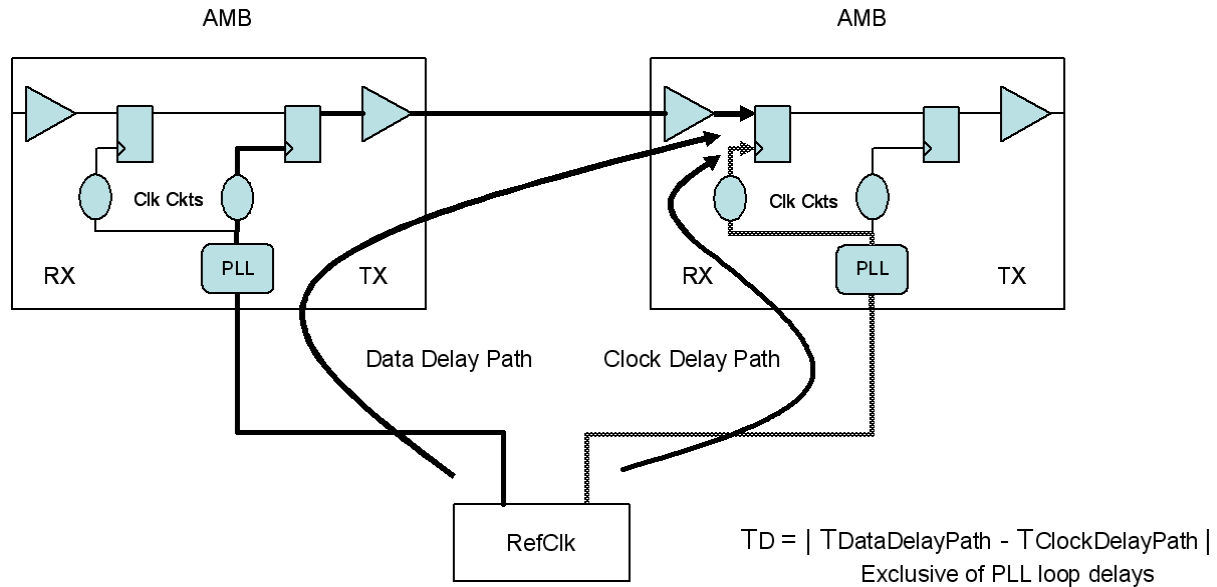


Figure 4.9 — Definition of Transport Delay

4.2 Common Specifications between Transmitter and Receiver

4.2.1 ESD Support

All signals and power pins shall withstand 2000 V of ESD using the human body model and 500 V of ESD using the charged device model without damage. Class 2 per JEDEC JESD22-A114.

4.2.2 Short Circuit Requirements

The transmitter and receiver must be capable of withstanding a short circuit to ground of D+ and D- for a minimum of one second.

4.2.3 Hot Insertion and Removal

System implementations that support hot insertion and removal will likely have independent power supplies for the host and AMBs in the channel. Transmitters and receivers therefore must meet the following requirements (where “support” means that the component is not damaged by the operation):

- 1) FBDIMM transmitters and receivers must support loss of device power without prior notice.
- 2) FBDIMM transmitters and receivers must support power-down of an adjacent AMB in the FBDIMM channel without prior notice.
- 3) FBDIMM transmitters and receivers must support power-up of an adjacent AMB in the FBDIMM channel without prior notice.

NOTE Fully Buffered DIMMs are not required to support module insertion and removal while power is applied to the module socket.

4.2 Common Specifications between Transmitter and Receiver (cont'd)

4.2.4 Mode of Coupling

All TX-RX links must be DC coupled.

4.2 Common Specifications between Transmitter and Receiver (cont'd)

4.2.5 TX and RX Terminations

The TX and RX pins shall obey the return loss specifications in Table 4.3 and Table 4.4 for continuous transmission operation.

During port calibration the transmitter and receiver resistance must be set to meet the specifications in Table 4.3 and Table 4.4. The exact implementation is design specific.

4.2.6 TX and RX PLL Requirements

The TX and RX PLLs shall obey the bandwidth and jitter peaking specifications in Table 4.2 for continuous transmission operation.

Table 4.2 — PLL Specification for TX and RX

Symbol	Parameter	Min	Max	Units	Notes
$F_{\text{PLL-BW_TX-RX}}$	-3dB bandwidth (3.2 and 4.0 Gb/s link speeds)	11	33	MHz	1
$F_{\text{PLL-BW_TX-RX-4.8}}$	-3dB bandwidth (4.8 Gb/s link speed)	11	22	MHz	2
$\text{JitPk}_{\text{TX-RX}}$	Jitter Peaking	0.5	3	dB	3

NOTE 1 This implies a natural frequency ω range from $5.92 \cdot 2\pi$ to $17.7 \cdot 2\pi$ as assumed in Table 4.1.

NOTE 2 This implies a natural frequency ω range from $5.92 \cdot 2\pi$ to $11.8 \cdot 2\pi$ as assumed in Table 4.1.

NOTE 3 This implies a damping factor ζ of 0.54 as assumed in Table 4.1.

4.3 Differential Transmitter Output Specifications

4.3.1 Transmitter Output Compliance Eye

This specification defines a differential current mode driver with a three different TX voltage swing modes (large, regular and small). It is mandatory for all AMBs to support all three voltage swing modes. Support for more than one voltage swing mode for a host is optional.

The specification defines several de-emphasis settings for each voltage swing. Support for all defined de-emphasis settings is mandatory for all FBDIMM agents. Each setting is defined as a separate differential eye diagram that must be met for the transmitter.

4.3 Differential Transmitter Output Specifications (cont'd)

4.3.1 Transmitter Output Compliance Eye (cont'd)

Figure 4.10 defines the non-de-emphasized and de-emphasized eye heights for the large, regular and small voltage swing. The non-de-emphasis voltages are for a transition bit while the other voltages are for a de-emphasized bit. The values for $V_{TX-Eq-MinLt}$, $V_{TX-Eq-DIFFp-p-MIN}$, and $V_{TX-Eq-MaxLt}$ can be calculated by applying the minimum, nominal, and maximum de-emphasis ratios in Table 4.3 to the measured value of $V_{TX-DIFFp-p}$.

All eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. All eyes must meet the minimum timing requirement of $T_{TX-Eye-MIN}$, which is defined in Table 4.3. The eye diagrams must be valid for the entire duration of the TX test pattern specified in Section 5. An appropriate average transmitter UI must be used as the interval for measuring the eye diagram. The eye diagram is created using all edges of the specified TX test pattern.

The transmitter output eye is referenced to VSS and all transmitter terminations must be referenced to VSS.

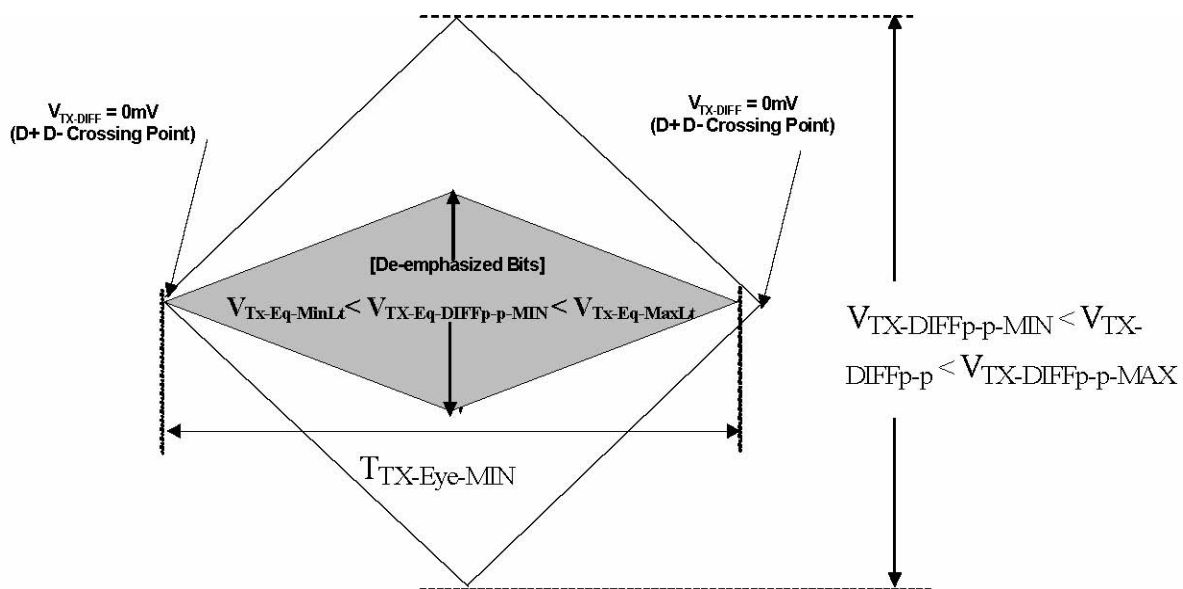


Figure 4.10 — Transmitter Output Eye Specifications, with and without De-emphasis

4.3 Differential Transmitter Output Specifications (cont'd)

4.3.1 Transmitter Output Compliance Eye (cont'd)

Figure 4.11 illustrates the transmitter timing specifications.

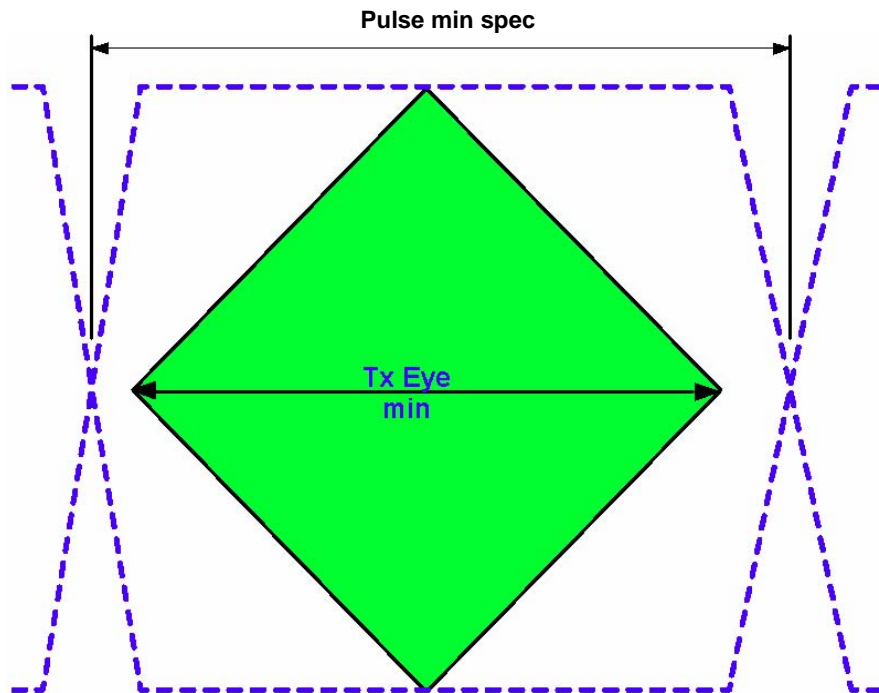


Figure 4.11 — Illustration of Timing Specification at TX

4.3 Differential Transmitter Output Specifications (cont'd)

4.3.1 Transmitter Output Compliance Eye (cont'd)

Figure 4.12 illustrates the de-emphasized string of patterns at the output of a transmitter

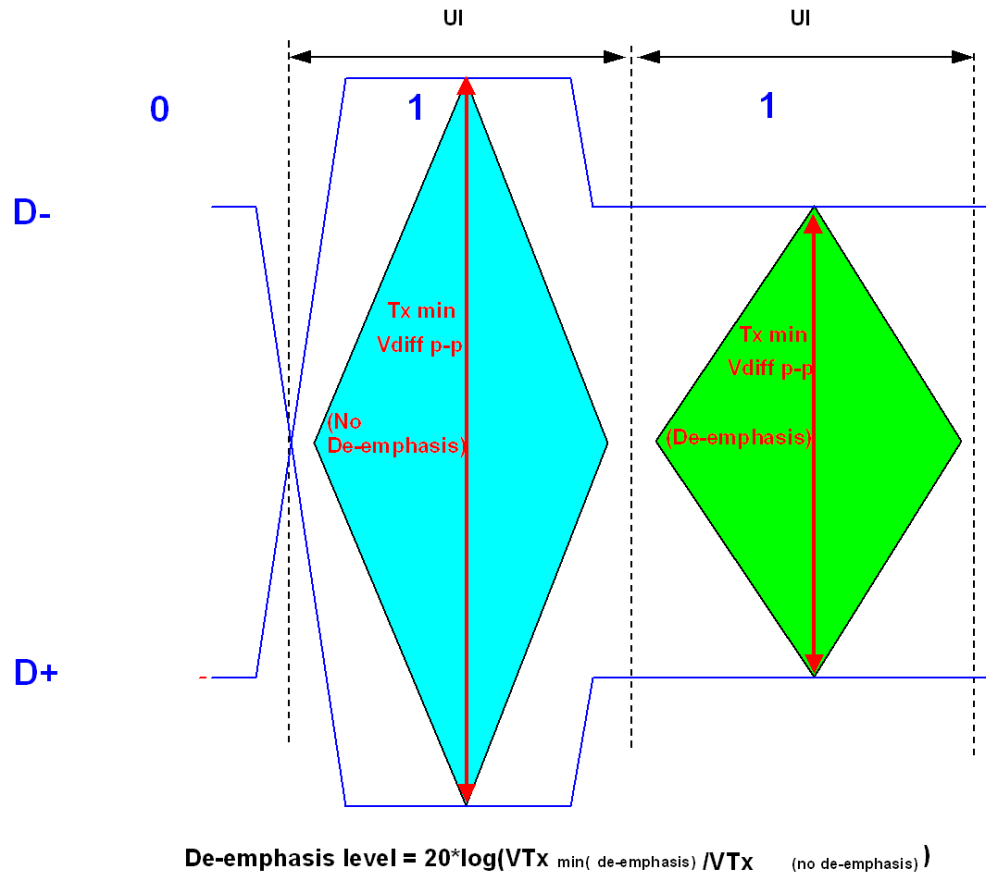


Figure 4.12 — Illustration of De-emphasis

4.3.2 Transmitter Lane to Lane UI Specification

Every lane of the TX must have the same average UI.

4.3 Differential Transmitter Output Specifications (cont'd)

4.3.3 Summary of Transmitter Output Specifications

Table 4.3 — Summary of Differential Transmitter Output Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Comments
$V_{TX-DIFFp-p_L}$	Differential peak-to-peak output voltage for large voltage swing	900	1300	mV	$V_{TX-DIFFp-p} = 2 * V_{TX-D+} - V_{TX-D-} $ Measured as Note 1
$V_{TX-DIFFp-p_R}$	Differential peak-to-peak output voltage for regular voltage swing	800		mV	$V_{TX-DIFFp-p} = 2 * V_{TX-D+} - V_{TX-D-} $ Measured as Note 1
$V_{TX-DIFFp-p_S}$	Differential peak-to-peak output voltage for small voltage swing	520		mV	$V_{TX-DIFFp-p} = 2 * V_{TX-D+} - V_{TX-D-} $ Measured as Note 1
V_{TX-CM_L}	DC common code output voltage for large voltage swing		375	mV	Defined as: $V_{TX-CM} = DC(avg)$ of $ V_{TX-D+} + V_{TX-D-} /2$ Measured as: Note 1
V_{TX-CM_S}	DC common mode output voltage for small voltage swing	135	280	mV	Defined as: $V_{TX-CM} = DC(avg)$ of $ V_{TX-D+} + V_{TX-D-} /2$ Measured as: Note 1 See also Note 2
$V_{TX-DE-3.5-Ratio}$	De-emphasized differential output voltage ratio for -3.5 dB de-emphasis	-3.0	-4.0	dB	1, 3, 4
$V_{TX-DE-6.0-Ratio}$	De-emphasized differential output voltage ratio for -6 dB de-emphasis	-5.0	-7.0	dB	1, 3, 4
$V_{TX-CM-ACp-p_L}$	AC peak-to-peak common mode output voltage for large swing		90	mV	$V_{TX-CM-AC} = Max V_{TX-D+} + V_{TX-D-} /2 - Min V_{TX-D+} + V_{TX-D-} /2$ Measured as: Note 1 See also Note 5
$V_{TX-CM-ACp-p_R}$	AC peak-to-peak common mode output voltage for regular swing		80	mV	$V_{TX-CM-AC} = Max V_{TX-D+} + V_{TX-D-} /2 - Min V_{TX-D+} + V_{TX-D-} /2$ Measured as: Note 1 See also Note 5
$V_{TX-CM-ACp-p_S}$	AC peak-to-peak common mode output voltage for small swing		70	mV	$V_{TX-CM-AC} = Max V_{TX-D+} + V_{TX-D-} /2 - Min V_{TX-D+} + V_{TX-D-} /2$ Measured as: Note 1 See also Note 5
$V_{TX-IDLE-SE}$	Maximum single-ended voltage in EI condition, DC + AC		50	mV	6, 7

4.3.3 Summary of Transmitter Output Specifications (cont'd)

Table 4.3 — Summary of Differential Transmitter Output Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Comments
$V_{TX-IDLE-SE-DC}$	Maximum single-ended voltage in EI condition, DC only		20	mV	6, 7, 8
$V_{TX-IDLE-DIFFp-p}$	Maximum peak-to-peak differential voltage in EI condition		40	mV	7
V_{TX-SE}	Single-ended voltage (w.r.t. VSS) on D+/D	-75	750	mV	1, 9
$T_{TX-EYE-MIN}$	Minimum TX eye width	0.7		UI	1, 10, 11
$T_{TX-DJ-DD}$	Maximum TX deterministic jitter		0.2	UI	1, 10, 11, 12
$T_{TX-PULSE}$	Instantaneous pulse width	0.85		UI	13
$T_{TX-RISE},$ $T_{TX-FALL}$	Differential TX output rise/fall time	30	90	ps	Given by 20%-80% voltage levels. Measured as: Note 1
$T_{TX-RF-MISMATCH}$	Mismatch between rise and fall times		20	ps	
$RL_{TX-DIFF}$	Differential return loss	8		dB	Measured over 0.1 GHz to 2.4 GHz. See also Note 14
RL_{TX-CM}	Common mode return loss	6		dB	Measured over 0.1 GHz to 2.4 GHz. See also Note 14
R_{TX}	Transmitter termination resistance	41	55	Ω	15
$R_{TX-Match-DC}$	D+/D- TX resistance difference		4	%	$RTX-Match-DC = 2 * RTX-D+ - RTX-D- / (RTX-D+ + RTX-D-)$ Bounds are applied separately to high and low output voltage states
$L_{TX-SKEW 1}$	Lane-to-lane skew at TX		100 + 3UI	ps	16, 18
$L_{TX-SKEW 2}$	Lane-to-lane skew at TX		100 + 2UI	ps	17, 18
$T_{TX-DRIFT-RESYNC}$	Maximum TX Drift (resync mode)		240	ps	19
$T_{TX-DRIFT-RESAMPLE}$	Maximum TX Drift (resample mode only)		120	ps	19
BER	Bit Error Ratio		10^{-12}		20

4.3.3 Summary of Transmitter Output Specifications (cont'd)

Table 4.3 — Summary of Differential Transmitter Output Specifications (NOTES)

NOTE 1 Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a 101010 pattern.

NOTE 2 The transmitter designer should not artificially elevate the common mode in order to meet this specification.

NOTE 3 This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.

NOTE 4 De-emphasis shall be disabled in the calibration state.

NOTE 5 Includes all sources of AC common mode noise.

NOTE 6 Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition.

NOTE 7 Specified at the package pins into a voltage compliance test load. Transmitters must meet both single-ended and differential output EI specifications.

NOTE 8 This specification, considered with $V_{RX-IDLE-SE-DC}$, implies a maximum 15 mV single-ended DC offset between TX and RX pins during the electrical idle condition. This in turn allows a ground offset between adjacent FBDIMM agents of 26 mV when worst-case termination resistance matching is considered.

NOTE 9 The maximum value is specified to be at least $(V_{TX-DIFFp-p} L / 4) + V_{TX-CM L} + (V_{TX-CM-ACp-p} / 2)$

NOTE 10 This number does not include the effects of SSC or reference clock jitter.

NOTE 11 These timing specifications apply to resync mode only.

NOTE 12 Defined as the dual-dirac deterministic jitter as described in Section 5.

NOTE 13 Pulse width measured at 0 V differential.

NOTE 14 One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.

NOTE 15 The termination small signal resistance; tolerance across voltages from 100 mV to 400 mV shall not exceed $\pm 5 \Omega$ with regard to the average of the values measured at 100 mV and at 400 mV for that pin.

NOTE 16 Lane to Lane skew at the Transmitter pins for an end component.

NOTE 17 Lane to Lane skew at the Transmitter pins for an intermediate component (assuming zero Lane to Lane skew at the Receiver pins of the incoming PORT).

NOTE 18 This is a static skew. An FBDIMM component is not allowed to change its lane to lane phase relationship after initialization.

NOTE 19 Measured from the reference clock edge to the center of the output eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.

NOTE 20 BER per differential lane. Refer to Section 5 for a complete definition of Bit Error Ratio.

4.4 Differential Receiver Input Specifications

The receiver definition starts from the input pin of the receiver end package and therefore includes the package and the receiver end chip.

4.4.1 Receiver Input Compliance Eye Specification

Following the specification of the transmitter, the receiver is specified in terms of the minimum input eye that must be maintained at the input to the receiver, and under which the receiver must function at the specified data rates.

The receiver eye is referenced to VSS and all input terminations at the receiver must be referenced to VSS. This input eye must be maintained for the entire duration of the RX test pattern. An appropriate average transmitter UI must be used as the interval for measuring the eye diagram. The eye diagram is created using all edges of the RX test pattern. The relationship between $T_{RX-Eye-MIN}$ shown in Figure 4.13 and $T_{RX-TJ-MAX}$ in Table 4.3 is described in 5.8.

The eye diagrams shall be measured by observing a continuous pattern at the pin of the device. Receiver test patterns are defined in 5.3.4.

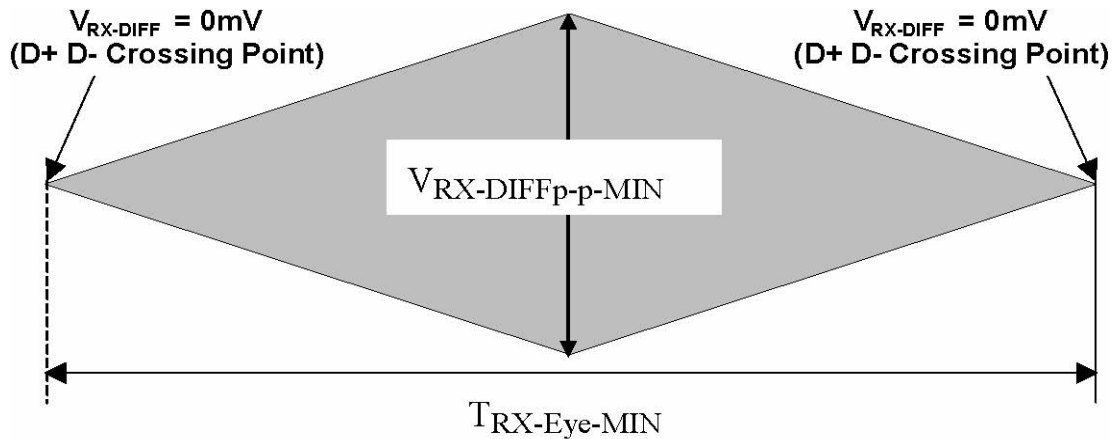


Figure 4.13 — Receiver Input Eye Voltage and Timing Specification

4.4.2 Summary of Receiver Input Specifications

Table 4.4 — Summary of Differential Receiver Input Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Comments
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	170	1300	mV	$VRX-DIFFp-p = 2* VRX-D+ - VRX-D- $ Measured as: Note 1
$V_{RX-IDLE-SE}$	Maximum single-ended voltage for EI condition (AC + DC)		65	mV	2, 3, 4, 5
$V_{RX-IDLE-SE-DC}$	Maximum single-ended voltage for EI condition (DC only)		35	mV	2, 3, 4, 5, 6
$V_{RX-IDLE-DIFFp-p}$	Maximum peak-to-peak differential voltage for EI condition		65	mV	3, 4, 5
V_{RX-SE}	Single-ended voltage (w.r.t. VSS) on D+/D	-300	900	mV	4
$V_{RX-DIFF-PULSE}$	Single-pulse peak differential input voltage	85		mV	4, 7
$V_{RX-DIFF-ADJ-RATIO-HI}$	Amplitude ratio between adjacent symbols, $1100\text{ mV} < VRX-DIFFp-p \leq 1300\text{ mV}$		3.0		4, 8
$V_{RX-DIFF-ADJ-RATIO}$	Amplitude ratio between adjacent symbols, $VRX-DIFFp-p \leq 1100\text{ mV}$		4.0		4, 8
$T_{RX-TJ-MAX}$	Maximum RX inherent timing error		0.4	UI	4, 9, 10
$T_{RX-DJ-DD}$	Maximum RX inherent deterministic timing error		0.3	UI	4, 9, 10, 11
$T_{RX-PW-ZC}$	Single-pulse width at zero-voltage crossing	0.55		UI	4, 7
$T_{RX-PW-ML}$	Single-pulse width at minimum-level crossing	0.2		UI	4, 7
$T_{RX-RISE},$ $T_{RX-FALL}$	Differential RX input rise/fall time	50		ps	Given by 20%-80% voltage levels.
V_{RX-CM}	Common mode of the input voltage	120	400	mV	Defined as: $VRX-CM = DC(aveg) \text{ of } VRX-D+ + VRX-D- /2$ Measured as: Note 1 See also Note 12

4.4.2 Summary of Receiver Input Specifications (cont'd)

Table 4.4 — Summary of Differential Receiver Input Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Comments
$V_{RX-CM-ACp-p}$	AC peak-to-peak common mode of input voltage		270	mV	$VRX-CM-AC = \text{Max } VRX-D+ + VRX-D- /2 - \text{Min } VRX-D+ + VRX-D- /2$ Measured as: Note 1
$V_{RX-CM-EH-Ratio}$	Ratio of $VRX-CM-ACp-p$ to minimum $VRX-DIFFp-p$		45	%	13
$RL_{RX-DIFF}$	Differential return loss	9		dB	Measured over 0.1GHz to 2.4GHz. See also Note 14
RL_{RX-CM}	Common mode return loss	6		dB	Measured over 0.1GHz to 2.4GHz. See Also Note 14
R_{RX}	RX termination resistance	41	55	Ω	15
$R_{RX-Match-DC}$	D+/D- RX resistance difference		4	%	$RRX-Match-DC = 2 * RRX-D+ - RRX-D- / (RRX-D+ + RRX-D-)$
$L_{RX-PCB-SKEW}$	Lane-to-lane PCB skew at Rx		6	UI	Lane-to-lane PCB skew at the receiver that must be tolerated. See also Note 16
$T_{RX-DRIFT}$	Minimum RX Drift Tolerance	400		ps	17
F_{TRK}	Minimum data tracking 3 dB bandwidth	0.2		MHz	18
$T_{EI-ENTRY-DETECT}$	Electrical idle entry detect time		60	ns	19
$T_{EI-EXIT-DETECT}$	Electrical idle exit detect time		30	ns	
BER	Bit Error Ratio		10-12		20

4.4.2 Summary of Receiver Input Specifications (cont'd)

Table 4.4 — Summary of Differential Receiver Input Specifications (NOTES)

NOTE 1 Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.

NOTE 2 Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition. Worst-case margins are determined by comparing EI levels with common mode levels during normal operation for the case with transmitter using small voltage swing. See Figure 4.17 and Figure 4.18.

NOTE 3 Multiple lanes need to detect the EI condition before the device can act upon the EI detection.

NOTE 4 Specified at the package pins into a timing and voltage compliance test setup.

NOTE 5 Receiver designers may implement either single-ended or differential EI detection. Receivers must meet the specification that corresponds to the implemented detection circuit.

NOTE 6 This specification, considered with $V_{RX-IDLE-SE-DC}$, implies a maximum 15 mV single-ended DC offset between TX and RX pins during the electrical idle condition. This in turn allows a ground offset between adjacent FBDIMM agents of 26 mV when worst-case termination resistance matching is considered.

NOTE 7 See Figure 4.14 and Figure 4.15. The single-pulse mask provides sufficient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eye mask.

NOTE 8 See Figure 4.16. The relative amplitude ratio limit between adjacent symbols prevents excessive inter-symbol interference in the Rx. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.

NOTE 9 This number does not include the effects of SSC or reference clock jitter.

NOTE 10 This number includes setup and hold of the RX sampling flop.

NOTE 11 Defined as the dual-dirac deterministic timing error as described in Section 5.

NOTE 12 Allows for 15 mV DC offset between transmit and receive devices.

NOTE 13 The received differential signal must satisfy both this ratio as well as the absolute maximum AC peak-to-peak common mode specification. For example, if $V_{RX-DIFFp-p}$ is 200 mV, the maximum AC peak-to-peak common mode is the lesser of $(200 \text{ mV} * 0.45 = 90 \text{ mV})$ and $V_{RX-CM-ACp-p}$.

NOTE 14 One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.

NOTE 15 The termination small signal resistance; tolerance across voltages from 100 mV to 400 mV shall not exceed $\pm 5 \Omega$ with regard to the average of the values measured at 100 mV and at 400 mV for that pin.

NOTE 16 This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component driving the signal to the receiver. This is one component of the end-to-end channel skew in the AMB specification.

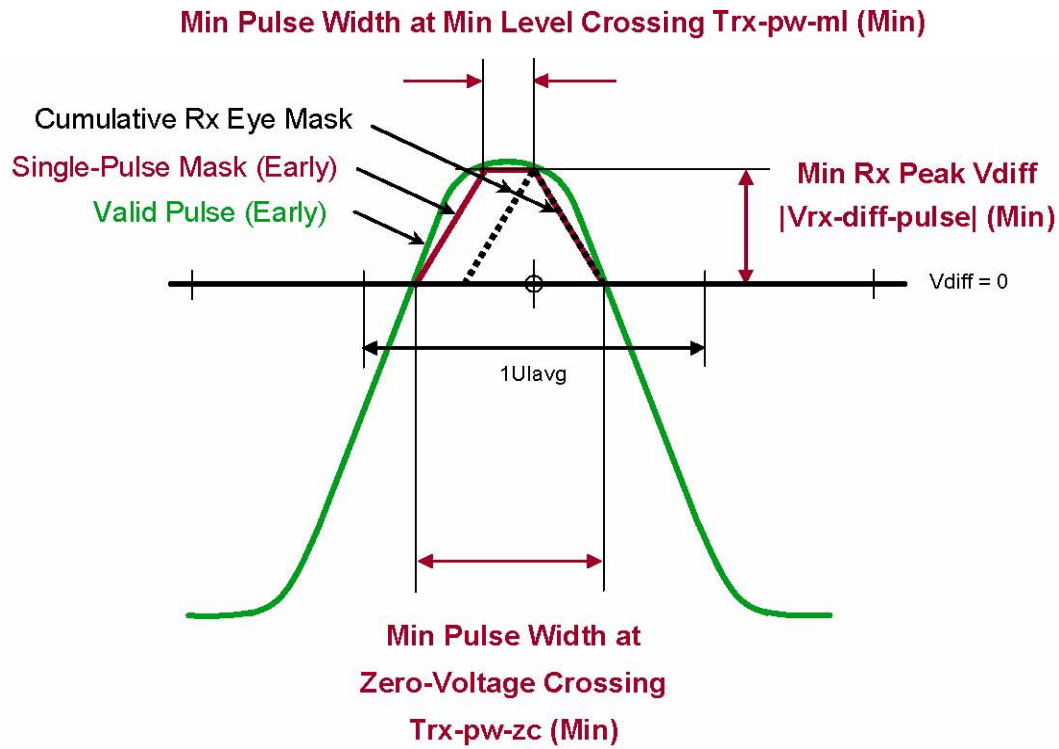
NOTE 17 Measured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.

NOTE 18 This bandwidth number assumes the specified minimum data transition density. Maximum jitter at 0.2 MHz is 0.05 UI, see Section 5 for full jitter tolerance mask.

NOTE 19 The specified time includes the time required to forward the EI entry condition.

NOTE 20 BER per differential lane. Refer to Section 5 for a complete definition of Bit Error Ratio.

4.4.2 Summary of Receiver Input Specifications (cont'd)



Pulse shifted early w.r.t. cumulative eye

Figure 4.14 — RX Single-Pulse Min Width and Amplitude Mask, Pulse Shifted Early

4.4.2 Summary of Receiver Input Specifications (cont'd)

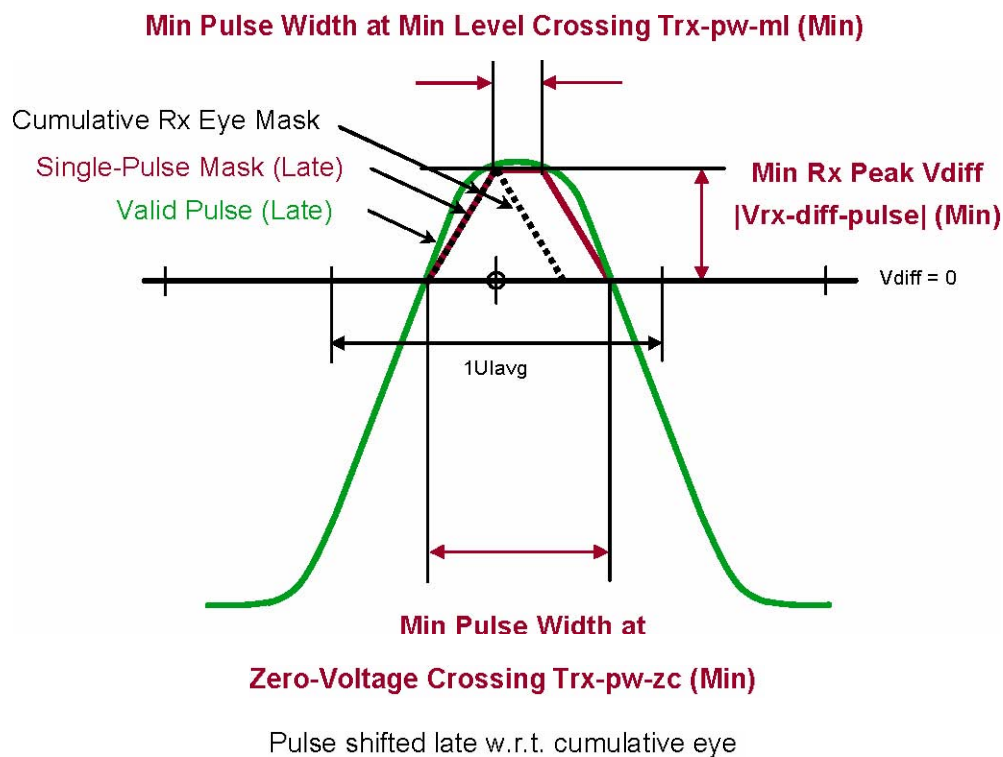


Figure 4.15 — RX Single-Pulse Min Width and Amplitude Mask, Pulse Shifted Late

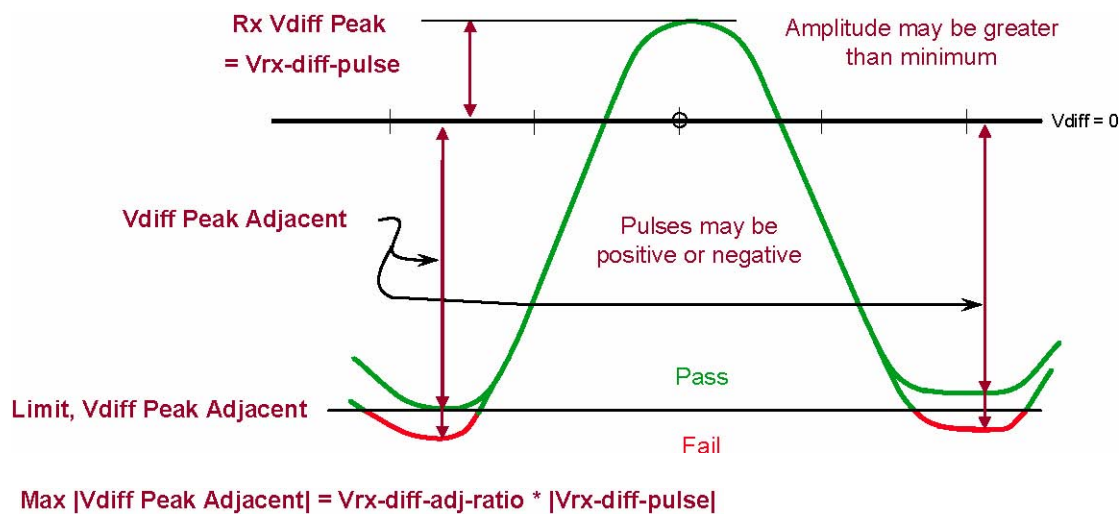


Figure 4.16 — RX Maximum Adjacent Symbol Amplitude

4.4.2 Summary of Receiver Input Specifications (cont'd)

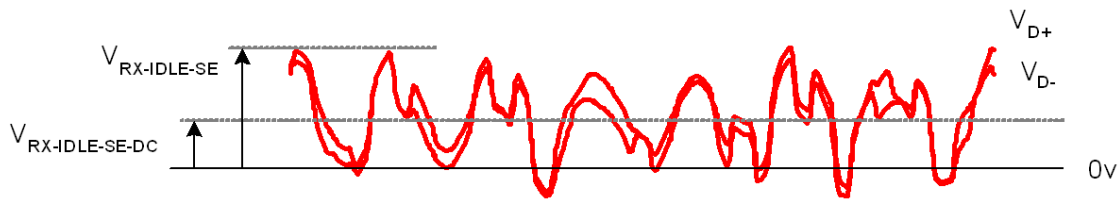


Figure 4.17 — RX Single-ended Electrical Idle Levels

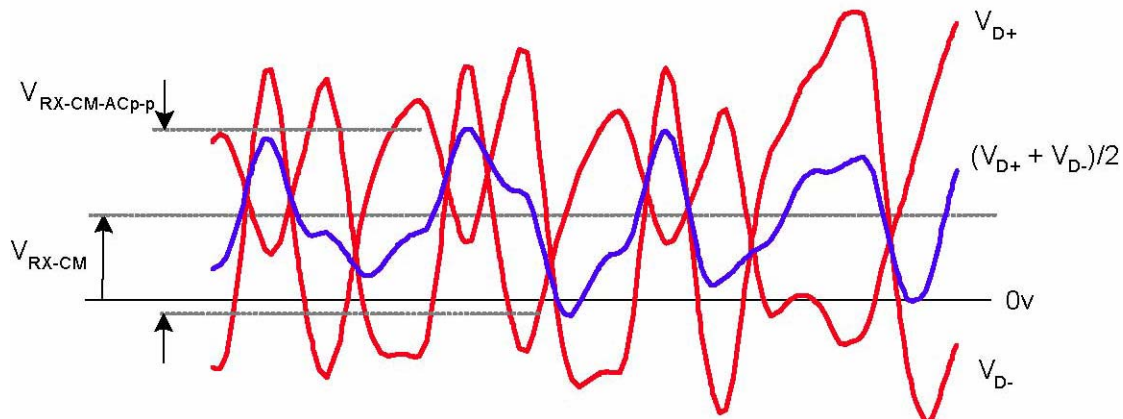


Figure 4.18 — RX Common Mode Levels during Normal Operation (Small Swing Setting)

5 Compliance Methodology

5.1 Introduction

This section describes the normative conditions under which an AMB or Host controller must be operating for conformance testing of the High Speed Point to Point Specification. This section should not be understood as recommendations for production testing, but as a Golden Methodology for compliance testing. It should be understood that all parameters are defined for TP_AMB, i.e., at the package ball of the DUT, and where appropriate, with respect to the electrically nearest ground ball. These sections are not to be understood as an exact laboratory procedure, but as a means to understanding the defined parameters in the specification.

5.2 Fundamentals of Jitter

5.2.1 Jitter

Jitter or phase noise, $\phi(t)$, is initially defined with respect to the phase, $S(t)$ of a periodic clock with frequency ω of units rad/sec, as:

$$S(t) = \omega t + \phi(t) \quad (5.1)$$

Jitter clearly has a spectral content. In this text, a jitter component is termed *wander* if its frequency is within the minimum bandwidth of the CDR present in the receiver, else it is termed *jitter*. In the FBDIMM system, wander is incurred through temperature and voltage variation, and Spread Spectrum Clocking. Given the low, 200kHz, bandwidth of the CDR, the transmitter, given a clean reference, is considered to have no significant wander components. To this end, no Golden PLL methodology is used, and the transmit jitter is contained from 0Hz to Nyquist.

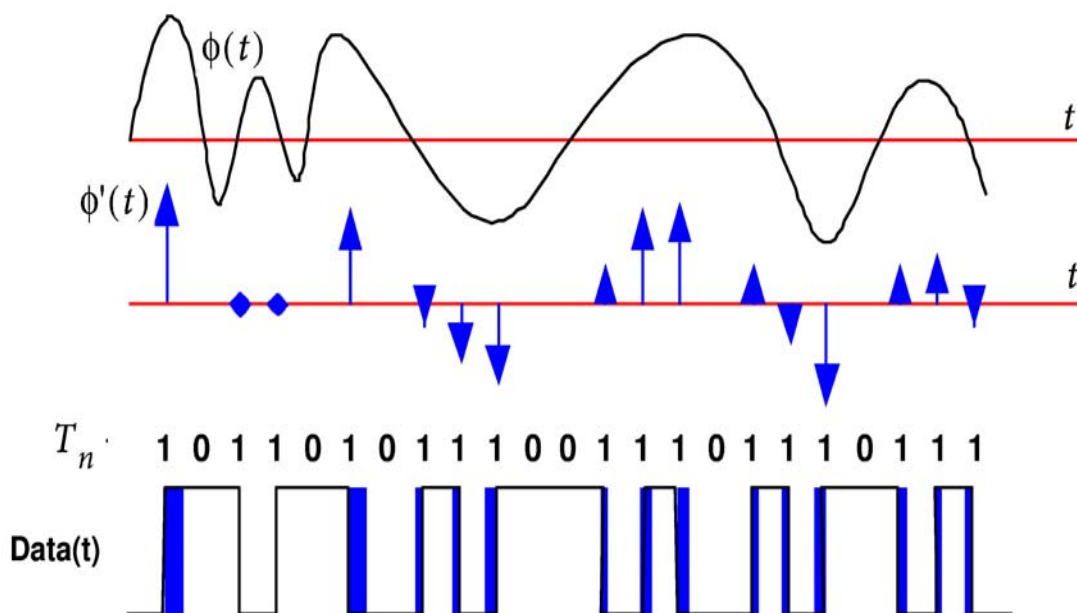


Figure 5.1 — Phase Noise as $\phi'(t)$ and $\phi(t)$

Given that the phase information is sampled only at the transition of the data stream; $T_n = \{0,1\}$ represents the occurrence of the transition, where zero represents no transition and one represents a transition. The jitter should be considered the convolution of deltas²

$$\phi'(t) = \sum_{n=1 \dots \infty} T_n \cdot \delta\left(t - n \frac{2\pi}{\omega}\right) \phi(t) \quad (5.2)$$

² Pertinent to Equation 5.2, it is perhaps noteworthy that the time errors, are negative when the phase noise is positive (i.e., advanced phase means negative time error, or the transition occurred before it was expected).

5.2 Fundamentals of Jitter (cont'd)

5.2.1 Jitter (cont'd)

It should be noted that T_n can represent any type of data transition e.g. correlated, periodic, or random.

Referring to Figure 5.2 and Figure 5.3 the probability density function, or histogram, $f(\Phi)$, of the jitter, Φ , can then be defined as the expected probability that the jitter achieves a given value.

$$f(\Phi) = \frac{\int_{-\infty}^{\infty} \delta(\phi'(t) - \Phi) dt}{\sum_{n=1}^{\infty} T_n} \quad (5.3)$$

This can then be extended to a cumulative density function (cdf), and noting that the cdf can be generated by integrating from both the left and right hand side and therefore has two sides. It should be noted that the cumulative distribution function, $F(\Phi)$, is actually the bit error ratio (BER) of a sampling process, sampling at Φ .

$$F_{\text{right}}(\Phi) = \int_{-\infty}^{\Phi} f(\phi) d\phi \quad (5.4)$$

$$F_{\text{left}}(\Phi) = \int_{\Phi}^{\infty} f(\phi) d\phi \quad (5.5)$$

It is assumed that the BER is only defined by either the left or right cdf. This assumption is not valid toward the middle of the eye, where the probability of both cdfs are of the same magnitude; however, given that this sampling point is not of interest to us, as the BER is negligible, this assumption is held true:

5.2 Fundamentals of Jitter (cont'd)

5.2.1 Jitter (cont'd)

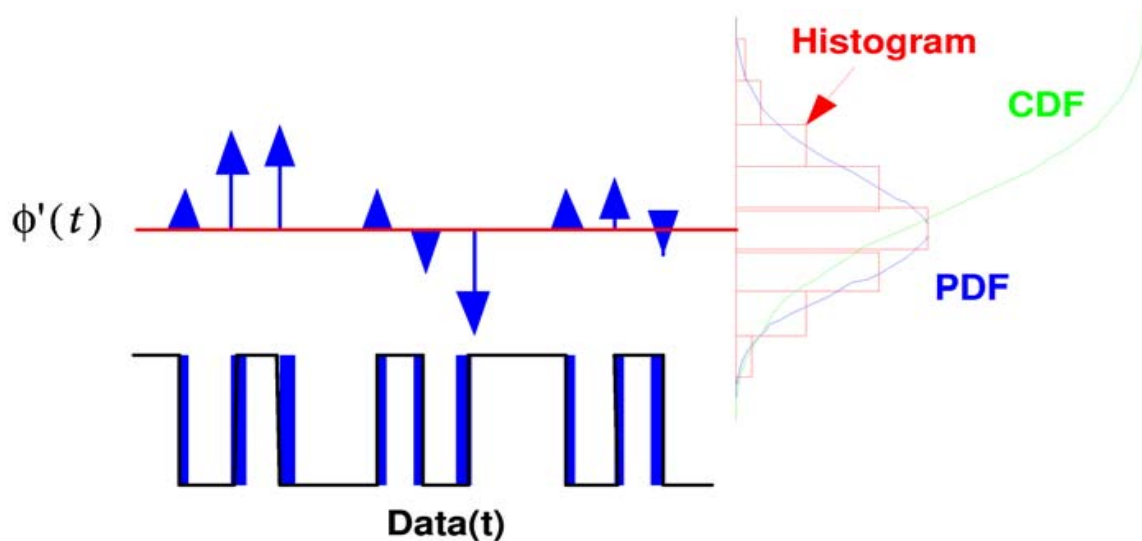


Figure 5.2 — Generation of a Cumulative Distribution Function from Time Domain Data

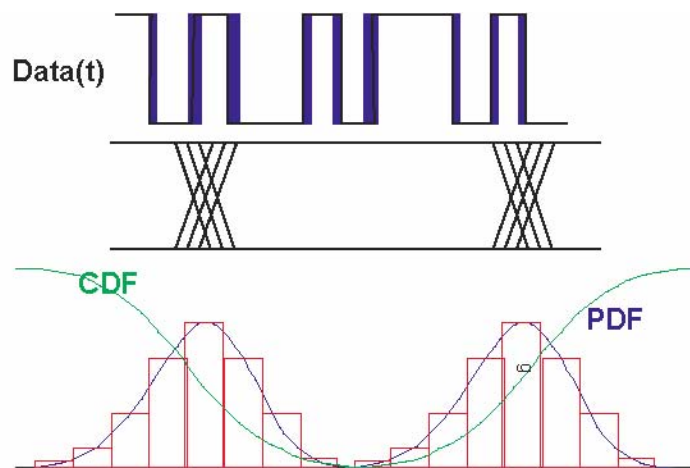


Figure 5.3 — Generation of a CDF from Time Domain Data (left and Right Side)

5.2.2 Dual Dirac Model

It should be understood that although jitter can be described using a dual Dirac model, it should not be understood that the jitter in the system really is dual Dirac. Typically jitter will be distributed or structured, and the dual Dirac description is merely the linearisation of the cdf at a particular BER. It should also be understood that the use of the dual Dirac model here and in the system budgeting is only a language to help define the jitter in the system, and does not imply that this be the normative derivation methodology for the derivation of the jitter in the system.

5.2 Fundamentals of Jitter (cont'd)

5.2.2 Dual Dirac Model

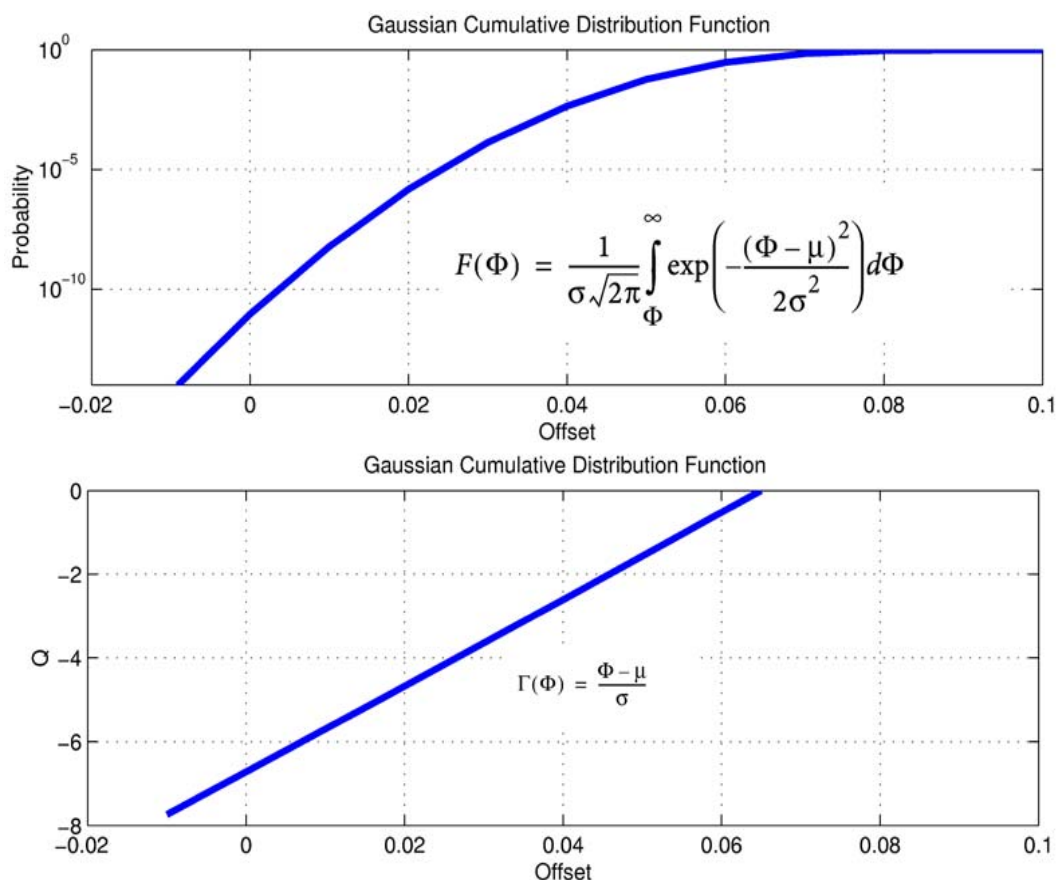


Figure 5.4 — Simple Gaussian Distribution using “BER” Units and “Q” Units

Referring to Figure 5.4, and assuming that the cumulative distribution function $F(\Phi)$ has a pure Gaussian distribution, we can write the cumulative distribution as³,

$$F(\Phi) = \frac{1}{\sigma\sqrt{2\pi}} \int_{\Phi}^{\infty} \exp\left(-\frac{(\Phi-\mu)^2}{2\sigma^2}\right) d\Phi \quad [\text{BER}] \quad (5.6)$$

³ Note that probability does not have any units normally. However, we will use units of BER to demonstrate a probability defined in terms of the frequency of occurrence.

5.2 Fundamentals of Jitter (cont'd)

5.2.2 Dual Dirac Model (cont'd)

This specific Gaussian distribution could also be written in units of Q, as

$$\Gamma(\Phi) = \frac{\Phi - \mu}{\sigma} \quad [Q] \quad (5.7)$$

This is clearly a linear function where $1/\sigma$ is the gradient and μ/σ is the offset from the origin. This mapping from $F(\Phi)$, in units of BER to $\Gamma(\Phi)$, in units of Q, is performed using the function

$$F(\Phi) = \frac{1}{\sigma\sqrt{2\pi}} \int_{\Phi}^{\infty} \exp\left(-\frac{\Gamma(\Phi)^2}{2}\right) d\Phi \quad [\text{BER}] \quad (5.8)$$

Using the definition of the error function

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-y^2} dy \quad (5.9)$$

we can rewrite the mapping as

$$F(\Phi) = 1 - \text{erf}\left(\frac{\Gamma(\Phi)}{\sqrt{2}}\right) \quad (5.10)$$

This inverse of this mapping can then be derived to give

$$\Gamma(\Phi) = \sqrt{2} \cdot \text{erf}^{-1}(1 - F(\Phi)) \quad (5.11)$$

This mapping now can be applied to an any arbitrary cumulative distribution function in units of BER. Clearly if the arbitrary cumulative distribution function is purely gaussian, then the resulting distribution $\Gamma(\Phi)$, can be simplified to the linear function (Equation 5.7). If the arbitrary function is a convolution of a structured bounded distributions and a gaussian distribution, Figure 5.5, then only a part (the tail) of the mapped distribution can be described by (Equation 5.7); however, this can be easily identified through the linearity.

5.2 Fundamentals of Jitter (cont'd)

5.2.2 Dual Dirac Model (cont'd)

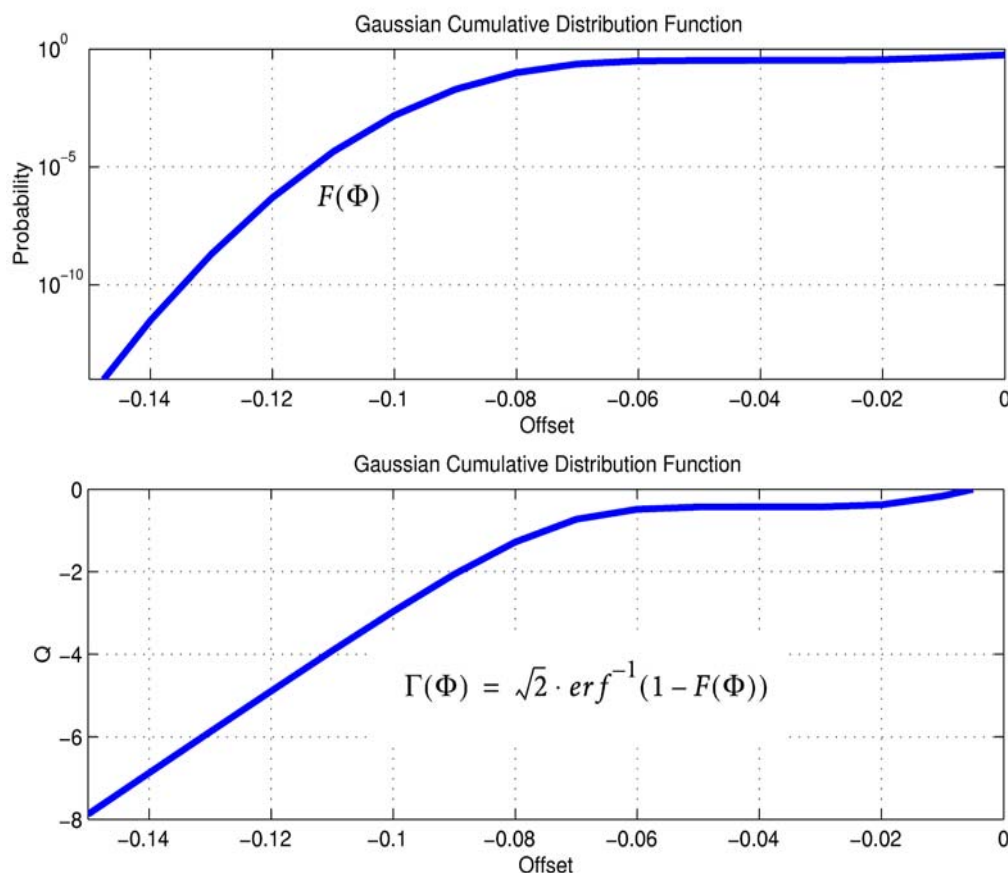


Figure 5.5 — Arbitrary Distribution using “BER” Units and “Q” Units

Using this mapping on the left and right cumulative distribution function defined above, Equation 5.4, Equation 5.5, we become the remapped distributions, $\Gamma_{\text{left}}(\Phi)$, and $\Gamma_{\text{right}}(\Phi)$, as shown in Figure 5.6.

The assumption that an arbitrary distribution will follow a gaussian distribution towards the tail of the distribution is fundamental to modeling of jitter in the system and is described by a so-called dual Dirac model, which consists of two Diracs convolved with a gaussian distribution, Figure 5.7. This distribution can also be described as two non-zero mean gaussian distributions and the probability density function as Equation 5.12. It is important to note that the defined pdf assumes that the two gaussian distributions have the same sigma, RJ_{dd} , which typically in reality is not true. However, as will be seen the derivation of RJ_{dd} , is based on the average on the two Gaussian distributions.

5.2 Fundamentals of Jitter (cont'd)

5.2.2 Dual Dirac Model (cont'd)

$$f(\Phi) = \frac{1}{2RJ_{dd}\sqrt{2\pi}} \left\{ e^{-\frac{(\Phi - k \cdot DJ_{dd})^2}{2RJ_{dd}^2}} + e^{-\frac{(\Phi + (1-k) \cdot DJ_{dd})^2}{2RJ_{dd}^2}} \right\} \quad (5.12)$$

where $0 < k < 1$ is an arbitrary value. DJ_{dd} and RJ_{dd} describe exactly the distribution and are referred to as the deterministic and random jitter components respectively. Although somewhat misleading this nomenclature is widely used, therefore through out this document to avoid confusion, random and deterministic will be written with the appropriate subscript, RJ_{dd} , DJ_{dd} . Given the remapped distributions $\Gamma_{left}(\Phi)$, and $\Gamma_{right}(\Phi)$, and referring to Figure 5.6 the dual dirac parameters DJ_{dd} and RJ_{dd} can be defined as shown in the following equations⁴:

$$RJ_{dd}(Q_{dd}) = \left(\left| \frac{\partial \Phi}{\partial \Gamma_{left}} \right| + \left| \frac{\partial \Phi}{\partial \Gamma_{right}} \right| \right) / 2 \quad (5.13)$$

$$DJ_{dd}(Q_{dd}) = \left[\Gamma_{right}^{-1}(Q_{dd}) - Q_{dd} \left| \frac{\partial \Phi}{\partial \Gamma_{right}} \right| \right] + \left[\Gamma_{left}^{-1}(Q_{dd}) - Q_{dd} \left| \frac{\partial \Phi}{\partial \Gamma_{left}} \right| \right] \quad (5.14)$$

where $\Gamma_{right}^{-1}(Q)$ and $\Gamma_{left}^{-1}(Q)$ are the inverse functions of $\Gamma_{left}(\Phi)$, and $\Gamma_{right}(\Phi)$

Note again that Equation 4.13 and Equation 4.14 are only defined for a specific point on the arbitrary distribution, i.e., at $\Gamma_{left}(\Phi) = \Gamma_{right}(\Phi) = Q_{dd}$.

⁴ If the left and right gradients, and are not within 10% of each other then the maximum of either value should be taken and not the average.

5.2 Fundamentals of Jitter (cont'd)

5.2.2 Dual Dirac Model (cont'd)

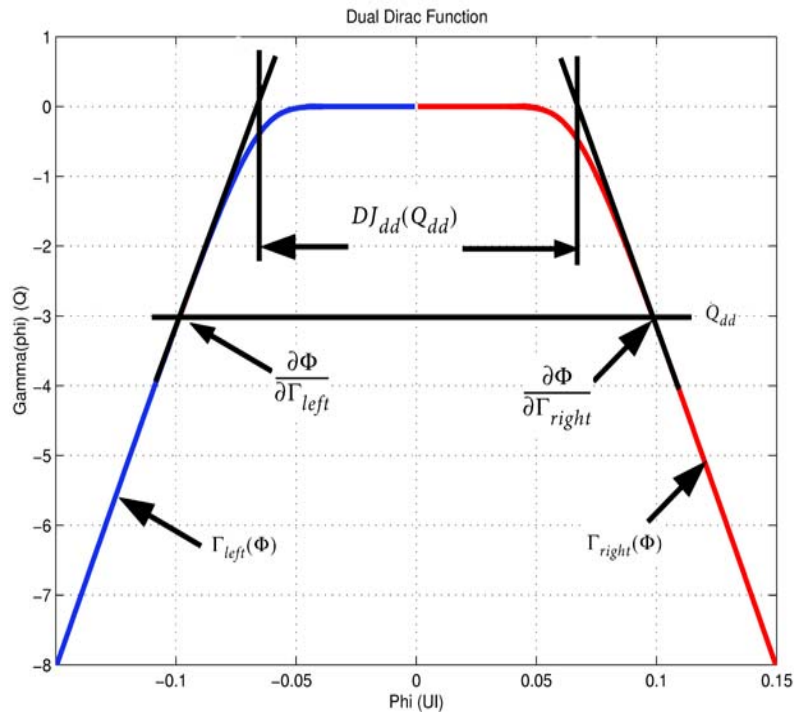


Figure 5.6 — CDF for Dual Dirac Model

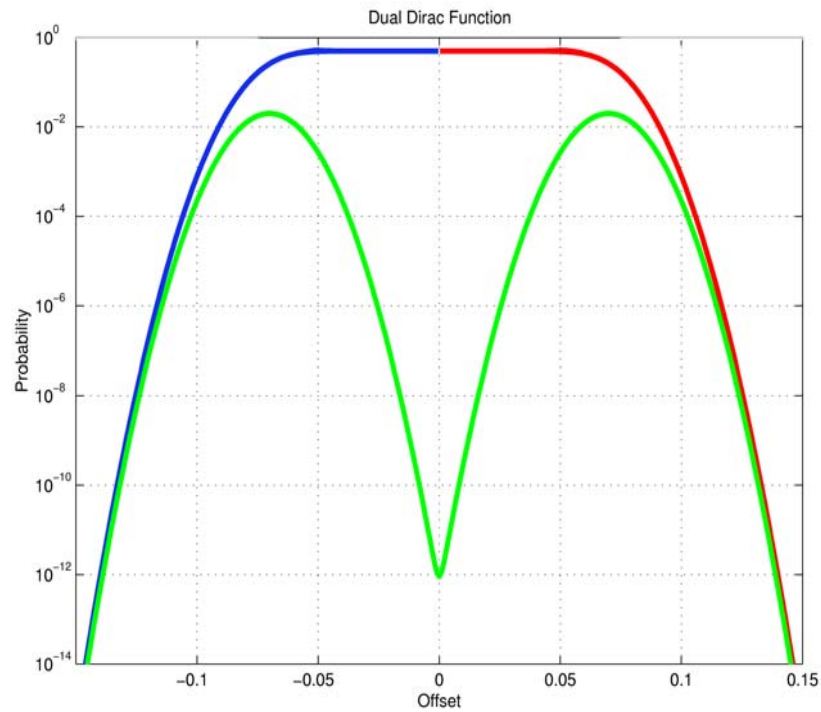


Figure 5.7 — PDF for Dual Dirac Model

5.3 High Speed Receiver

The follow condition shall be used for the validation of

- Receiver Sensitivity
- Receiver Inherent DJ/TJ Jitter

In the testing of a receiver, two types of tests have been defined to stress the receivers under the conditions typically seen in the application.

5.3.1 Calibration of Jitter

During the course of testing a receiver, a stressed signal must be calibrated by:

- Using enough multiple measurement to guarantee correct sampling of jitter frequency components below 1kHz
- Measuring or equivalently derived⁵ the CDF at points where $BER < 1e^{-9}$, or $Q > 6.0$.
- Estimating the TJ and DJ_{dd} , based on the dual Dirac model such that a signal not exceeding the target jitter is identified as such with a 99.7% confidence level.⁶

5.3.2 Long Channel

Using a clean reference clock (see 5.9), the device shall be brought into a mode equivalent to that in the final application. Equivalent means any functionality that effects the ability of the receiver to receive a BIST stream with a given BER, e.g., CDR power save, active MEMBIST, ripple power supply.

Referring to Figure 5.9, the LUT shall be driven by a phased modulated pattern generator. It is assumed that the phased modulator is band limited enough such that DJ modulation actually gives a uniformly distributed jitter output.

- All other CALs shall be active as defined and either the LUT or CAL phase shifted so as to give the worst case crosstalk relationship.
- The LUT input shall be initially calibrated to the defined RJ_{dd} and DJ_{dd} as described in Table 5.1 Jitter Tolerance w/o channel. Referring to Figure 5.8, and using a reasonable frequency step, a sinusoidal modulation shall then be added at a single frequency for the entire mask defined, with the corresponding amplitude. A triangular 32 kHz fundamental modulation with amplitude defined in 4.1.3 shall also be added to represent the residual SSC modulation.
- The signal shall then be passed through a electrical channel, such that an additional data correlated jitter, as defined in Table 5.1, Channel is added to the signal.

⁵ It is not necessary to determine the cdf. This language is only used to enable the requirements of the measurement to be defined.

⁶ For confidence interval calculations, the jitter distribution can be assumed to be the convolution of an unbounded Gaussian distribution with a finite number of uncorrelated delta functions, and a bounded even distribution. In the calculation of any confidence interval, the inherent measurement error and noise of the instrument must be taken into account.

5.3 High Speed Receiver (cont'd)

5.3.2 Long Channel (cont'd)

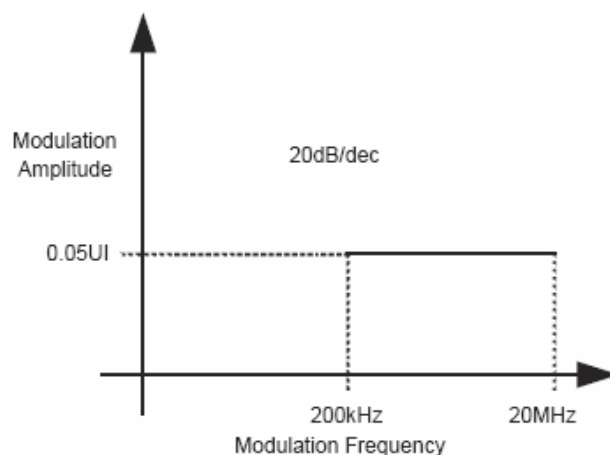


Figure 5.8 — Sinusoidal Modulation Profile

Please note that the channel is only present to introduce DDJ and shape the signal, and does not represent the actual channel in the system e.g., inducing crosstalk.⁷ The common mode noise source shall be adjusted to the defined maximum receiver common mode noise. The amplitude at the transmitter shall be adjusted so as to give the defined minimum receiver accumulated amplitude

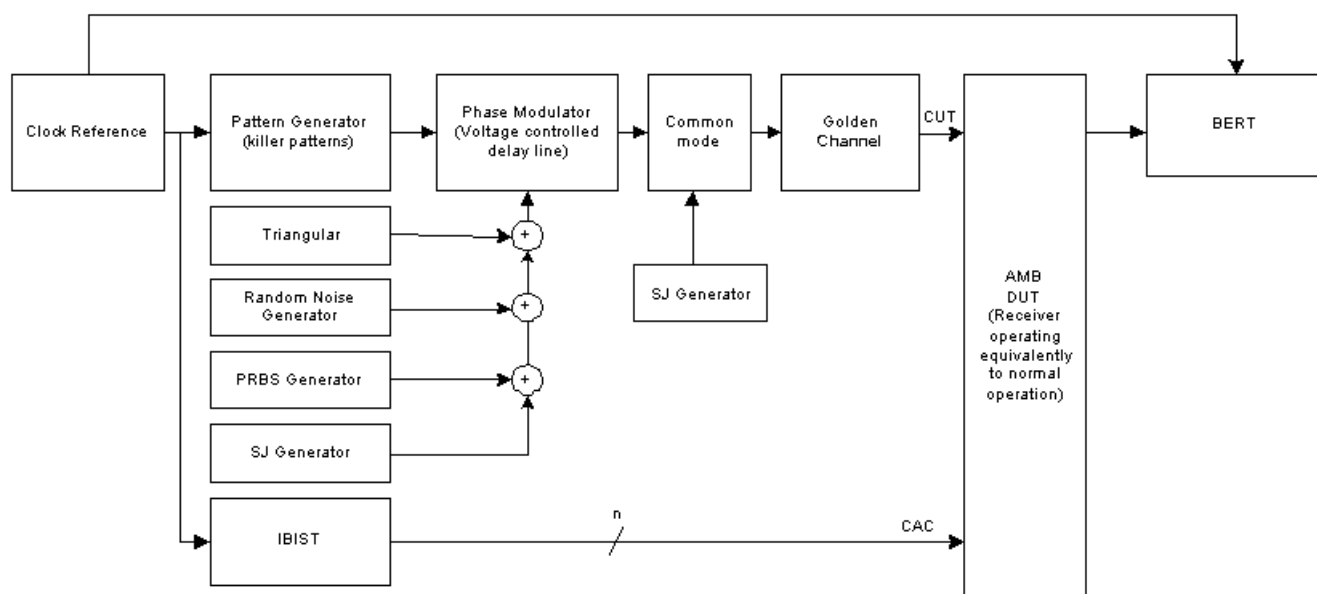


Figure 5.9 — Long Channel Receiver Compliance Test Setup

⁷ It is currently being considered whether a form of de-emphasis or boosting can be used at the transmitter to give more realistic signals at the receiver under test.

5.3 High Speed Receiver (cont'd)

5.3.3 Short Channel

Using a clean reference clock (see 5.9), the device shall be brought into a mode equivalent to that in the final application. Equivalent means any functionality that affects the ability of the receiver to receive a BIST stream with a given BER, e.g., CDR power save, active MEMBIST, ripple power supply.

Referring to Figure 5.10, the LUT shall be driven by a phased modulated pattern generator. It is assumed, that the phased modulator is band limited enough such that DJ modulation actually gives a uniformly distributed jitter output.

- All other CALs shall be active as defined and either the LUT or CAL phase shifted so as to give the worst case crosstalk relationship.
- The LUT input shall be initially calibrated to the defined RJ_{dd} and DJ_{dd} as defined in Table 5.1, Jitter Tolerance w channel. A triangular 32kHz fundamental modulation with amplitude defined in 4.1.2 shall also be added to represent the residual SSC modulation.
- Referring to Figure 5.8, and using a reasonable frequency step, a sinusoidal modulation shall then be added at a single frequencies for the entire mask defined, with the corresponding amplitude.
- The signal shall then be passed through a short channel, such that the edge rate at the receiver is at the maximum defined.
- The amplitude at the transmitter should be adjusted to the minimum transmit amplitude.
- The differential noise source should adjusted so as to give the defined minimum receiver amplitude⁸.

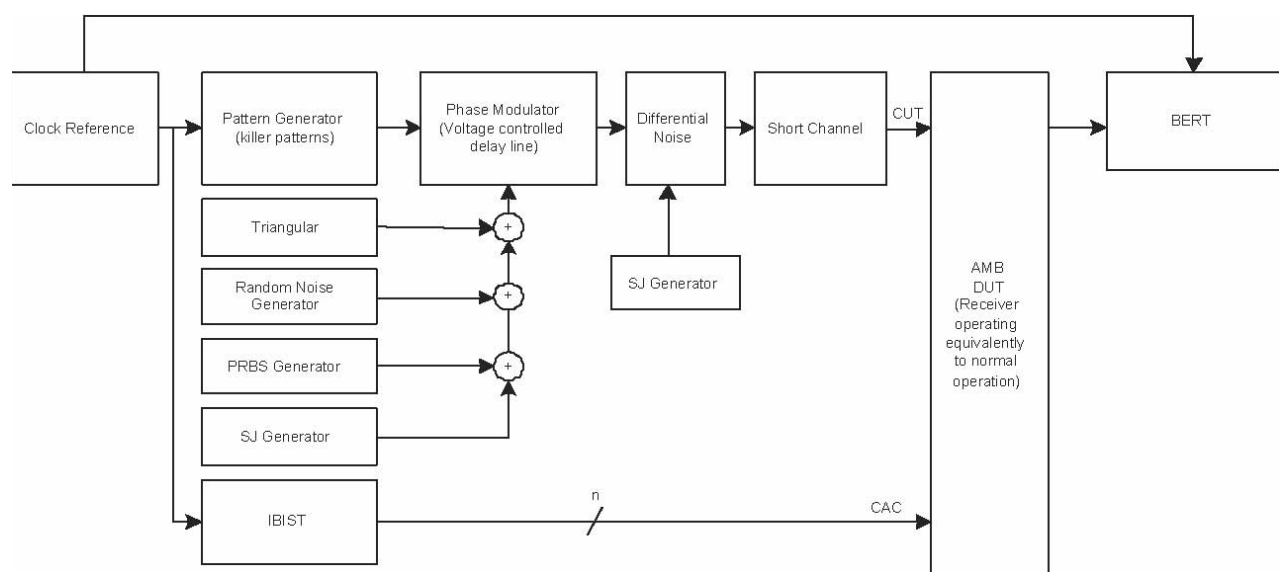


Figure 5.10 — Short Channel Receiver Compliance Test Setup

⁸ It is currently being investigated how the minimum pulse requirements can be fulfilled with this setup

5.3 High Speed Receiver (cont'd)

5.3.4 Patterns

The LUT shall be tested exhaustively using all of the following patterns⁹:

1. 42 x Clock[0xaaa] + 1 x User[0x001000]
2. 42 x Clock[0xaaa] + 1 x User[0x123456]
3. 42 x Clock[0xaaa] + 1 x User[0xcccccc]

A LUT, implementing continuous CDR tracking shall also exhaustively use all of the following patterns:

1. 42 x Clock[0xfc0] + 1 x User[0x001000]
2. 42 x Clock[0xfc0] + 1 x User[0x123456]
3. 42 x Clock[0xfc0] + 1 x User[0xcccccc]
4. PRBS31

All CAL transmitters shall transmit:

1. $m \times \text{Clock}[0xccc] + n \times \text{Constant}[0x000]$
where m and n should be adjusted to simulate any package resonances.
2. 1 x Clock[0xaaa]
with all possible inversion permutations on the CUT physically, significantly to the LUT.
3. PRBS31

Inversion permutations imply that the worst case superposition of multiple aggressors is not known and therefore each possible combination must be tried.

Each combination of LUT and CAL patterns shall be run repetitively until a statistically significant measurement can be made.

5.3.5 Measurement

At each of the defined conditions, the BER of the LUT should be estimated. To enable a confident BER to be measured the TJ shall be increased beyond the requirements of the system, by increasing the RJ content. From multiple BER measurements for varying TJ the BER, for the system defined TJ, shall be estimated such that a device exceeding the TJ or DJ requirements is identified as such with a 99.7% confidence level.

$$Q_n = \sqrt{2} \cdot \text{erf}^{-1}(1 - \text{BER}_n)$$

$$1.0 = \text{DJ}_{\text{cal}_n} + \text{DJ}_{\text{rx}} + Q_n(\text{RJ}_{\text{cal}_n} + \text{RJ}_{\text{rx}}) \quad (5.15)$$

This can be further understood referring to Equation 5.15. Given multiple applied jitter, DJ_{cal_n} and RJ_{cal_n} we measure a bit error rate for the DUT of BER_n .

Given a dual dirac model, there must exist an inherent jitter for the receiver DJ_{rx} and RJ_{rx} for which Equation 5.15 holds true. This relationship is only a simplified model and typically will only be true for operation points where the BER is similar.

⁹ All patterns are defined using terminology that is used to control the IBIST, as defined in the AMB DFX Specification

5.4 High Speed Transmitter

The following conditions shall be used for the validation of

- Transmit Common mode
- Transmit Eye
- Transmit Jitter

5.4.1 Clean Condition

Using a clean reference clock (see 5.9), all activity and noise that may effect the behavior of the transmitter should be eliminated. Only the LUT shall drive the defined pattern, with all CALs disabled.

5.4.2 Realistic Condition

Using a clean reference clock (see 5.9), the device must be brought into a mode equivalent to that in the final application. Equivalent means any functionality that effects the performance of the transmitter, e.g., active MEMBIST, ripple power supply. The LUT shall drive the defined pattern, while all other CALs are active.

5.4.3 Clean Patterns

The LUT shall transmit the following pattern¹⁰:

1. 1 x clock[0xccc]

5.4.4 Realistic Patterns

The LUT shall be tested exhaustively using the following pattern and their inverse:

1. 41 x Constant[0x000] + 1 x User[0x001000] + 1 x Clock[0x333]
2. 41 x User[0x167167] + 1 x Clock[0x333]
3. 41 x User[0x123456] + 1 x Clock[0x333]
4. PRBS31

All CAL receivers and transmitters shall transmit exhaustively each of the following, in combination with all the LUT test patterns:

1. 1 x Clock[0xaaa]
with all possible inversion permutations on the CUT physically, significantly close to the LUT.
2. m x Clock[0xccc] + n x Constant[0x000]
3. PRBS31

Inversion permutations imply that the worst case superposition of multiple aggressors is not known and therefore each possible combination must be tried.

Each combination of LUT and CAL patterns shall be run repetitively until a statistically significant measurement can be made.

¹⁰ All patterns are defined using terminology that is used to control the IBIST, as defined in the AMB DfX Specification

5.4 High Speed Transmitter (cont'd)

5.4.5 Measurement

Referring to Figure 5.11, in order to avoid the overestimation of RJ from the transmitter, the measurement shall be performed in two steps.

1. Using the 'Realistic' conditions and patterns described above, the TJ shall be estimated by
 - Using enough multiple measurements to guarantee correct sampling of jitter frequency components below 1 kHz.
 - Measuring or equivalently derived¹¹ the CDF at points where $BER < 10^{-9}$
 - Extrapolating Φ to a $BER < 10^{-9}$, such that a device exceeding the TJ specification is identified as such with a 99.7% confidence interval.¹²
2. Using the 'clean' conditions and patterns, the DJ shall be estimated by
 - Using enough multiple measurement to guarantee correct sampling of jitter frequency components below 1 kHz
 - Measuring or equivalently deriving the CDF at points where $BER < 10^{-6}$
 - Extrapolate the estimated TJ, using a derived RJ_{dd} from the measurements to give a DJ_{dd} , such that a device exceeding the DJ specification is identified as such with a 99.7% confidence level.¹³

¹¹ It should be understood that the CDF need not be derived. This language is only used to enable a definition of the requirements.

¹² For confidence interval calculations, the jitter distribution can assumed to be the convolution of an unbounded Gaussian distribution with a finite number of uncorrelated delta functions, and a bounded even distribution. In the calculation of any confidence interval, the inherent measurement error and noise of the instrument must be taken into account.

¹³ Please note that variation of the accuracy of the measurement can be made to re-examine a failing part, to ensure that the percentage of good devices identified as being bad is also decreased.

5.4 High Speed Transmitter (cont'd)

5.4.5 Measurement (cont'd)

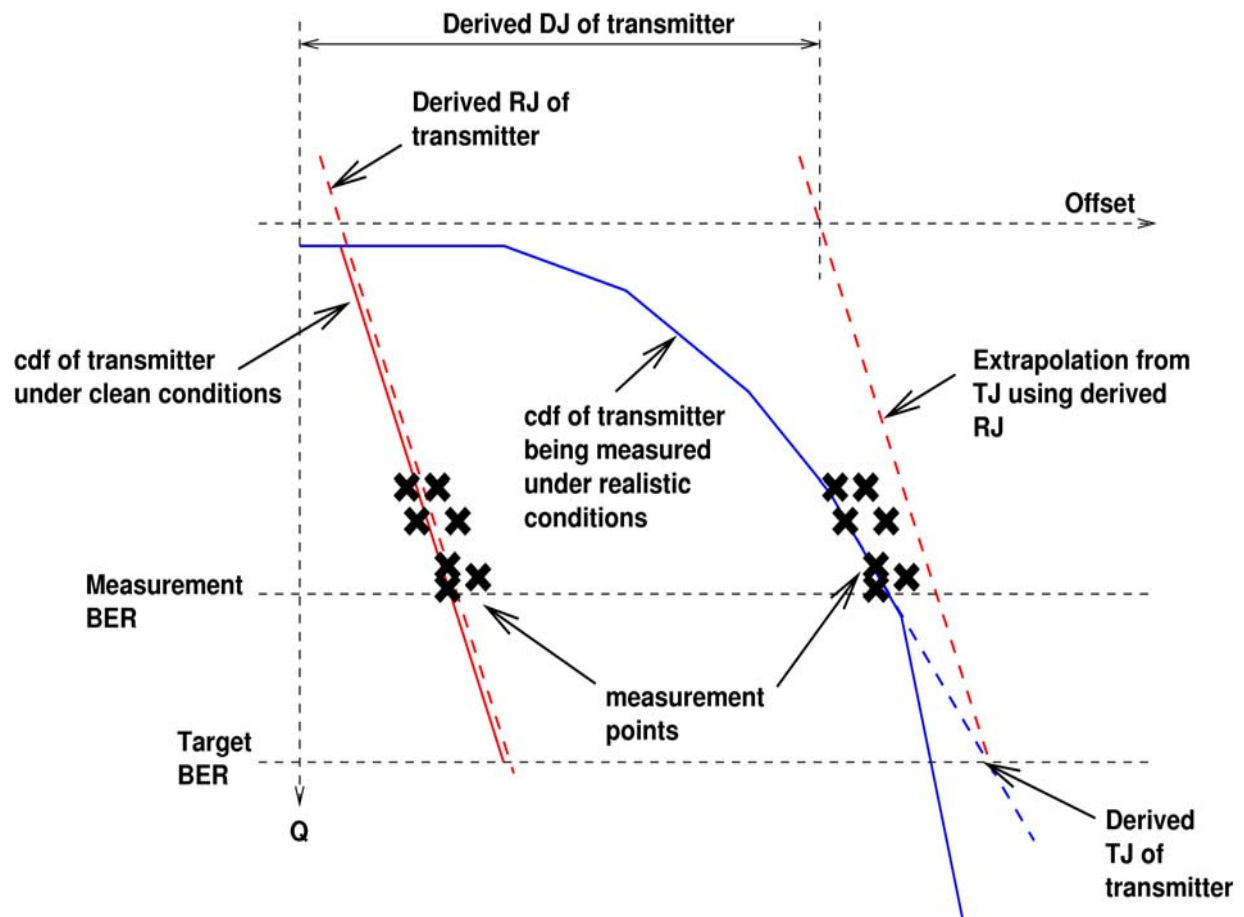


Figure 5.11 — Transmit Jitter Extrapolation of DJ_{dd} , RJ_{dd} , and TJ

5.5 Low Speed Transmitter

For compliance testing of de-emphasis transmit amplitudes the following patterns should be used¹⁴:

1. 1 x UserPattern[0x0f3355]

5.6 Reference Clock

Referring to Figure 5.12, the reference clock shall be measured by taking direct time samples of the reference clock, calculating the time samples of the transients, and applying the defined PLL difference function. At least 10^9 samples shall be taken, and the all the harmonics of the SSC shall be initially removed from the filtered time records before calculating the rms value.

¹⁴ All patterns are defined using terminology that is used to control the IBIST, as defined in the AMB DFx Specification.

5.6 Reference Clock (cont'd)

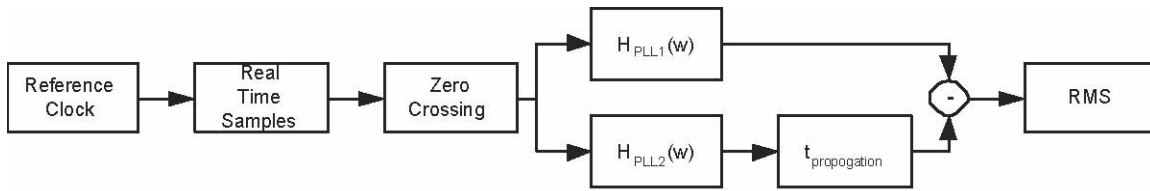


Figure 5.12 — Reference Clock Measurement Configurations

5.7 PLL Transfer Function

The PLL transfer verification should be understood as a comparison of the DUT's PLL characteristics to the expected ideal PLL characteristic used for the measurement of the reference clock. Ideally, the PLL would have a linear 2nd order response, with given bandwidth range and peaking range, to any input signal. In reality it is known that PLLs are only approximated by this response for complex jitter input signals, and therefore the difference must be determined.

Initially a clock reference is required that just¹⁵ meets the required reference clock specification. It is recommended that a production reference buffer be taken in order to achieve a realistic jitter spectrum. Given that this reference should be within specification, it should be necessary to add additional white noise to the output signal in order to increase the rms phase noise, such that it is just within the specification, a.k.a a calibrated rusty reference.

Using this calibrated rusty reference the assumed theoretical PLL response, used in the measurement of the reference clock, can be verified by measuring both the output of the PLL and the reference clock, and building the difference function. This difference function should be performed in the exactly the same way as for the reference clock measurement, except that one of the PLL responses is substituted by the real output of the PLL under test. Clearly some care must be taken concerning skew in the measurements, and the inherent noise of the DUT PLL must be removed from the final rms jitter. Each of the four possible combinations of PLL bandwidth and propagation delay should be checked to ensure that the worst case is identified.

Given, the resulting rms value is less than the initially measured reference clock, no further action need be taken. If the resulting rms value is larger, then the rms difference must be rms added to the inherent receiver and transmitter jitter.

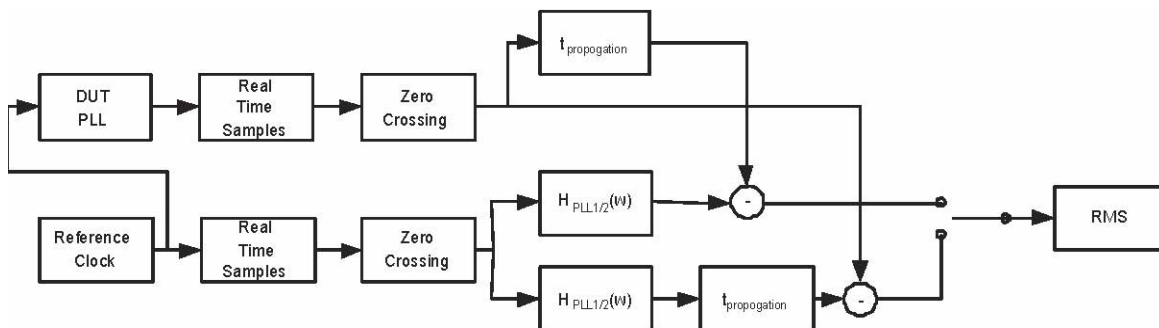


Figure 5.13 — PLL Measurement Configurations

¹⁵ "Just" should be understood from a practical engineering standpoint and being as close as realistically possible to the maximum allowed.

5.8 Jitter Budget Explanation

Referring to the informative jitter budget in Table 5.1¹⁶, the budget is designed to support interoperability of devices from all AMB suppliers within different system implementations, so each component is considered to introduce a maximum amount of jitter to the system. In the FBDIMM application four components are identified and allocated a maximum amount of TJ and DJ_{dd}. Note that a dual Dirac model is assumed for system allocated allowing RJ_{dd} components to be added rms, and DJ_{dd} component linearly. For the system to operate at a given BER or better, the total sum of DJ_{dd} and RJ_{dd} multiplied by the appropriate 2Q must be less than 1.0 UI. The eye opening at the transmitter can be considered to be T_{TX-Eye-MIN}, i.e., the total jitter seen at the transmitter is 1 - T_{TX-Eye-MIN}. Of this total jitter, T_{TX-DJ-DD}, is the allowed maximum deterministic jitter.

The sampling jitter inherent in the receiver is defined as T_{RX-TJ-MAX}, of which T_{TX-DJ-DD} is the maximum deterministic. This inherent jitter can be understood in terms of the maximum deterministic jitter that can be applied to the receiver for the given target BER, i.e., 1 - T_{RJ-TJ-MAX}. In reality, however, due to the rms addition of RJ_g, the maximum jitter that can be applied to the receiver is the dual Dirac sum of all the other jitter sources in the system. Referring to Table 5.1, the maximum jitter that can be tolerated is TJ_{JitterTolerance} with 1 - TJ_{JitterTolerance} being the minimum open eye, T_{RX-Eye-MIN}, that can be received in the system.

Table 5.1 — Jitter Budget

	RJ (σ_{UI})	RJ (UI _{tot})	DJ(UI _{tot})	SJ(UI _{tot})	TJ(UI _{tot})
TX	0.007	0.100	0.200 T _{TX-DJ-DD}		0.300 1 - T _{TX-Eye-MIN}
RX	0.007	0.100	0.300 T _{RX-DJ-DD}		0.400 T _{RX-TJ-MAX}
Reference Clock Induced Jitter	0.012 T _{REF_JITTER_RMS}	0.170			0.170
Channel			0.280		0.280
Total		0.220	0.780		1.000
Jitter Tolerance without channel	0.012	0.200	0.150	0.050	0.400
Jitter Tolerance with channel	0.012	0.200	0.430	0.050	0.680

5.9 “Clean” Reference Clock Input Specification

Validation of many AMB Tx and Rx specifications parameters requires that a “clean” reference clock be applied to the AMB. This section defines the characteristics of a clean reference clock for the purposes of validating compliance with the specification. The clean reference clock voltage level specifications in Table 5.2 describe the reference clock signal at the balls of the AMB. The settings of the signal generator creating the clean reference clock may therefore need to be adjusted depending on the characteristics of the cabling and fixturing connecting the generator to the AMB and whether the AMB under test employs on-die reference clock termination.

¹⁶ Please refer to Section 4 for the normative parameters.

5.9 Clean” Reference Clock Input Specifications (cont’d)**Table 5.2 — Clean Reference Clock Input Specifications**

Symbol	Parameter	Min	Max	Units	Notes
$f_{\text{CleanRefclk-3.2}}$	Reference clock frequency @ 3.2 Gb/s (nominal 133.33 MHz)	$f_{\text{Refclk-3.2}}(\text{Min})$	$f_{\text{Refclk-3.2}}(\text{Max})$	MHz	1, 2
$f_{\text{CleanRefclk-4.0}}$	Reference clock frequency @ 4.0 Gb/s (nominal 166.67 MHz)	$f_{\text{Refclk-4.0}}(\text{Min})$	$f_{\text{Refclk-4.0}}(\text{Max})$	MHz	1, 2
$f_{\text{CleanRefclk-4.8}}$	Reference clock frequency @ 4.8 Gb/s (nominal 200 MHz)	$f_{\text{Refclk-4.8}}(\text{Min})$	$f_{\text{Refclk-4.8}}(\text{Max})$	MHz	1, 2
V_{CleanMax}	Single-ended maximum voltage		0.900	V	3, 5
V_{CleanMin}	Single-ended minimum voltage	-0.1		V	3, 6
$V_{\text{CleanRefclk-diff-ih}}$	Differential voltage high	500	600	mV	4
$V_{\text{CleanRefclk-diff-il}}$	Differential voltage low	-600	-500	mV	4
$V_{\text{CleanCross}}$	Absolute crossing point	250	550	mV	3, 7, 8
$V_{\text{CleanCross-delta}}$	VCross variation		20	mV	3, 7
$V_{\text{CleanRefclk-cm-acp-p}}$	AC common mode		20	mV	9
$ER_{\text{CleanRefclk-diff-Rise}}$ $ER_{\text{CleanRefclk-diff-Fall}}$	Rising and falling edge rates	3	4.0	V/ns	4, 10
$ER_{\text{CleanRefclk-Match}}$	% mismatch between rise and fall edge rates		5	%	3, 11
$T_{\text{CleanRefclk-Dutycycle}}$	Duty cycle of reference clock	49	51	%	4
$V_{\text{CleanRB-diff}}$	Ringback voltage threshold	-485	485	mV	4, 12
$T_{\text{CleanStable}}$	Allowed time before ringback	500		ps	4, 12
$N_{\text{CleanSAMPLE}}$		N_{SAMPLE}		periods	13
$T_{\text{CLEANREFBWLIMIT-RMS-JIT}}$	Reference clock total RMS jitter from 10Mhz to Nyquist		750	fs	15
$T_{\text{CLEANREF2ns_RMS-REL_JITr}}$	Total RMS relative jitter measured between the reference clock and a 2ns delayed copy of the reference clock.		750	fs	14, 15, 16
$T_{\text{CLEANREF-SSCp-p}}$	Reference clock jitter (peak-to-peak) due to spread spectrum clocking effects		0	ps	2

5.9 Clean Reference Clock Input Specifications (cont'd)

Table 5.2 — Clean Reference Clock Input Specifications (NOTES)

NOTE 1 The nominal reference clock frequency is determined by the data frequency of the link divided by 2 times the fixed PLL multiplication factor for the FBDIMM channel (6:1). $f_{data} = 2000$ MHz for a 4.0Gbps FBDIMM channel and so on.

NOTE 2 Spread spectrum clocking is not allowed.

NOTE 3 Measurement taken from single-ended waveform.

NOTE 4 Measurement taken from differential waveform. See Figure 4.1

NOTE 5 Defined as the maximum instantaneous voltage including overshoot. See Figure 4.3 in the Reference Clock Specification, using $V_{CleanMax}$ instead of V_{Max} .

NOTE 6 Defined as the minimum instantaneous voltage including undershoot See Figure 4.3 in the Reference Clock Specification, using $V_{CleanMin}$ instead of V_{Min} .

NOTE 7 Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 4.3 in the Reference Clock Specification.

NOTE 8 Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 4.3 in the Reference Clock Specification using $V_{CleanCross(Max/Min)}$ instead of $V_{Cross(Max/Min)}$.

NOTE 9 The majority of the reference clock AC common mode occurs at high frequency (i.e., the reference clock frequency).

NOTE 10 Measured from -150 mV to +150 mV on the differential waveform. The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential 0 V crossing. See Figure 4.5 in the Reference Clock Specification.

NOTE 11 Edge rate matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ± 75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK-falling. The median crosspoint is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations. The rising edge rate of REFCLK+ should be compared to the falling edge rate of REFCLK-. The maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 4.6 in the Reference Clock Specification.

NOTE 12 See Figure 4.7 in the Reference Clock Specification. T_{stable} is the time the differential clock must maintain a minimum $V_{CleanRefclk-diff-ih}$ or $V_{CleanRefclk-diff-il}$ differential voltage after rising / falling edges before it is allowed to droop back into the $V_{CleanRB-diff}$ differential range.

NOTE 13 Direct measurement of phase jitter records over N_{SAMPLE} periods may be impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and the total jitter at N_{SAMPLE} samples extrapolated from an estimate of the sigma of the random jitter components. For details on this measurement, refer to Section 5.6.

NOTE 14 This is the clean reference clock total RMS jitter within the jitter spectrum band ranging from 10MHz to Nyquist. This may be measured by a variety of techniques such as spectrum or phase noise analyzer, waveform capture and analysis, or any other technique that can isolate jitter components within the specified frequency band.

NOTE 15 A valid clean reference clock must simultaneously satisfy both $T_{CLEANREF-2ns_SELF-REL_JITr}$ and $T_{CLEANREF-BWLIMIT-RMSJIT}$.

NOTE 16 The $T_{CLEANREF-2ns_RMS-REL_JIT}$ is the jitter measurement indicated by the measurement instrument. It includes the relative jitter intrinsic to the reference clock itself as well as jitter elements added by the measurement fixturing and cabling, and the instrument itself. Instrument and fixture/cabling effects that can be characterized and removed automatically by the measurement algorithm are not included in this value.

5.9 Clean Reference Clock Input Specification (cont'd)

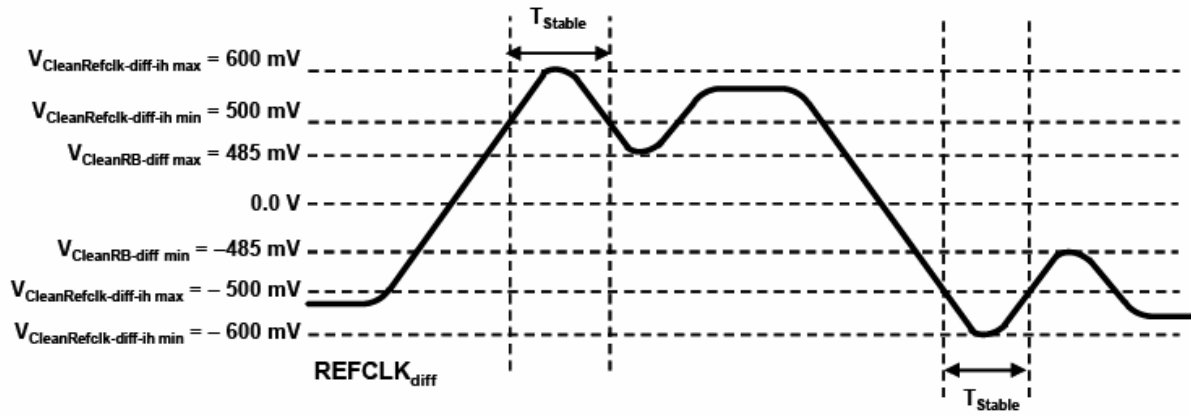


Figure 5.14 — Reference Clock measurement Configurations

Annex A (informative) Revision History

Version	Date	Changes
0.0 DRAFT	12/03/2003	Intermediate draft to JEDEC for comments only
0.1	2/04/2004	Initial JEDEC release
0.1a	2/19/2004	Incorporated changes based on internal and external review feedback
0.1b	2/26/2004	More editorial and numerical changes
0.1c	3/15/2004	Final version for April 2004 ballot
0.1d	4/15/2004	Editorial changes from April 2004 ballot comments
0.2	5/26/2004	Changes from TG discussion; non-consensus numbers in italics
0.2a	6/3/2004	Changes from initial Rev 0.2 review in TG
0.2b	7/15/2004	New consensus numbers approved, removed Section 4
0.3	9/10/2004	New consensus numbers approved, added detail to hot swap section
0.3a	9/30/2004	New consensus numbers approved, new specs added
0.3b	10/15/2004	New consensus numbers approved, editorial changes
0.3c	10/27/2004	New consensus numbers approved, editorial changes
0.4	11/5/2004	New consensus numbers approved, editorial changes
0.5	11/10/2004	Editorial changes
0.6	1/13/2005	Modifications / additions to reference clock table
0.6a	3/3/2005	Modifications / additions to reference clock table
0.6b	4/12/2005	Approved clarifications
0.7	5/10/2005	Approved clarifications plus consensus spec changes
0.8	8/14/2005	Approved clarifications plus consensus timing numbers for 4.8 Gb/s link speeds
0.8	12/15/2005	Added clean reference clock material per V&V ballot

Changes From Rev 0.8 to Rev 0.85

Added Section 4.9, which adds specifications for the “clean” reference clock referred to in various places in Section 4. The material was created and approved by the FBDIMM1 Validation and Verification task group.

Annex A (informative) Revision History (cont'd)

Changes From Rev 0.7 to Rev 0.8

Removed tracking bandwidth component of reference clock difference filter; added Tref-sscp-p at a value of 30 ps; added max PLL bandwidth of 22 MHz for 4.8 Gb/s link speeds; added minimum PLL peaking of 0.5 dB; removed TBD 4.8 Gb/s bin splits in Tables 3.3 and 3.4; various clarifications in Section 4; added PLL transfer method to Section 4.

Changes From Rev 0.6B to Rev 0.7

Reduced Vrx-ei-se and Vrx-ei-se-dc. Added footnotes to clarify system requirements for meeting single-ended electrical idle specifications. Corrected footnote numbering in Tables 3.1, 3-3, and 3-4. Editorial clarifications and typo corrections.

Changes From Rev 0.6A to Rev 0.6B

Expanded interconnect description to include DIMM and motherboard parameters used in task group simulations. Added clarifying language and figures for single-ended electrical idle margin analysis. Added footnotes to clarify TX and RX requirements for meeting single-ended and differential electrical idle specifications.

Changes From Rev 0.6 to Rev 0.6a

Reference clock table: Added Vmin and Vmax specs to limit overshoot and undershoot at the input; determined values for AC common mode and minimum slew rate (had been TBD); added footnote to AC common mode table entry.

Changes From Rev 0.5 to Rev 0.6

Reference clock table: replaced single-ended voltage level and rise/fall time specs with differential voltage and edge rate specs. Added crosspoint delta and ringback specs.

Changes From Rev 0.4 to Rev 0.5

Clarified Note 14 in Table 3.4. Editorial changes.

Changes From Rev 0.3D to Rev 0.4

Several numbers moved to consensus (non-italic). Modified adjacent pulse diagrams in RX footnotes. Changed BER to 10^{-12} throughout. Added Tref-jitter-delta, removed Tref-dj. Modified footnotes as appropriate. Changed all italicized values to TBD. Editorial changes.

Changes From Rev 0.3C to Rev 0.3D

Reference clock frequency moved to consensus (non-italic). Modified pulse width definitions in RX tables. Modified TX and RX termination measurement voltage. Changed Vrx-idle-se value. Added Vrx-diff-p-adj. Changed Vrx-diffp-p max to TBD. Editorial changes.

Annex A (informative) Revision History (cont'd)

Changes From Rev 0.3B to Rev 0.3C

Several numbers moved to consensus (non-italic). Added pulse height and width entries to RX tables. Added 1 second limit to short-circuit requirement. Modified CM specifications in TX and RX tables. Removed 9.5 dB pre-emphasis entry in TX table. Changed “eye height” to $V_{rx-diff-pin}$ RX table. Separated reference clock frequency specification into 3 entries, one for each nominal operating frequency. Editorial changes.

Changes From Rev 0.3A to Rev 0.3B

Several numbers moved to consensus (non-italic). Added BER entry to TX and RX tables. Changed name of TTX-Total-Min to TTX-Eye-Min, TRX-Total-Min to TRX-Eye-Min, and TRX-Total-Max to TRX-TJ-Max. Removed note 9 from TX table and note 8 from RX table. Editorial changes.

Changes From Rev 0.3 to Rev 0.3A

Several numbers moved to consensus (non-italic). Removed Nui-min specifications from TX and RX tables as well as references to same. Added single-ended EI RX DC specification and EI detect specifications. Separated TX CM AC specifications to correspond to the three levels of swing. Changed “termination impedance” to “termination resistance” throughout. Changed FBD references to FBDIMM. Modified footnotes as necessary.

Changes From Rev 0.2B to Rev 0.3

Several numbers moved to consensus (non-italic). Added detail to hot swap section. Added single-ended EI TX DC specification. Separated 4.8 Gb/s jitter specs from 3.2 and 4.0 Gb/s jitter specs.

Changes From Rev 0.2A to Rev 0.2B

Several numbers moved to consensus (non-italic). Removed Section 4 and references to Section 4. Added RX max ratio of input AC CM to eye height. Added drift and drift tolerance specs.

Changes From Rev 0.2 to Rev 0.2A

Changed designation of RX timings from jitter to “inherent timing error,” including note that this includes flop setup and hold times, specifications are now maximum values (rather than minimum eye openings); change to wording and diagrams in 3.4.1 will still be required. Corrected footnote numbering in Table 3.4. Added deterministic jitter to Table 3.1.

Annex A (informative) Revision History (cont'd)

Changes From Rev 0.1D to Rev 0.2

Added table entries for deterministic jitter and accompanying footnotes, all jitter in ps rather than UI. Removed minimum TX common mode specifications for large and regular swings, reduced minimum TX common mode for small swing. Added clarifying language to indicate that reference clock jitter is to be considered a separate jitter category apart from TX and RX jitter specifications. Added table entry for TX rise/fall mismatch. Minor editorial changes as agreed upon by the task group.

CHANGES FROM REV 0.1C TO REV 0.1D

In termination section, removed reference to high-impedance state and programmable termination impedance. Minor editorial changes.

CHANGES FROM REV 0.1B TO REV 0.1C

Added note that de-emphasis is disabled in calibration state. Added footnote with SSC reference to clock table. Added maximum single-ended and differential voltages in EI condition for TX and RX. Deleted EI detection threshold for RX. Minor editorial changes.

CHANGES FROM REV 0.1A TO REV 0.1B

Stated that -9.5dB setting is not required for small voltage swing mode; added receiver data tracking bandwidth spec; changed transmitter timing diagram drawing; changed location of reference clock spec from clock buffer output to reference clock input.

CHANGES FROM REV 0.1 TO REV 0.1a

Fixed incorrect -9.5dB de-emphasis spec; added PLL bandwidth table to Common TX/RX section; changed termination parameter names from Z to R; changed termination tolerancespecs; changed RX AC common mode voltage; removed compliance test pattern; allowed small undershoot in SE voltage specs; widened common mode voltage range for RX; minor editorial changes.

CHANGES FROM JEDEC FORMATTING FOR PUBLICATION AS JESD8-18

To conform with the JEDEC Manual, JM7, the following changes were made: Revision History moved to end and labeled Annex A, Section 1.3 and subclauses became Section 3, Section 3 became 4, Section 4 became 5. All references were updated to reflect changes in renumbering.



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